FAIRCHILD
SEMICONDUCTOR®

SPT9400

TRIPLE VIDEO DRIVER WITH Y/C & COMPOSITE OUTPUT

FEATURES

- Triple Video Line Driver Chip With Y/C Inputs
- Composite and Y/C Outputs
- R_L = 150 Ω (75 Ω Back-Terminated Cable)
- Internal Clamping and Bias Circuitry
- Power-Down Standby Mode
- Very Small 5.0 x 4.4 mm Package
- Low Power Dissipation: 168 mW
- 1 V_{P-P} Input Range
- 6 dB Voltage Gain
- Flat Response f_{IN} = 100 kHz to 10 MHz (typical)
- Crosstalk -40 dB (Typical)
- Single +5 Volt Power Supply

APPLICATIONS

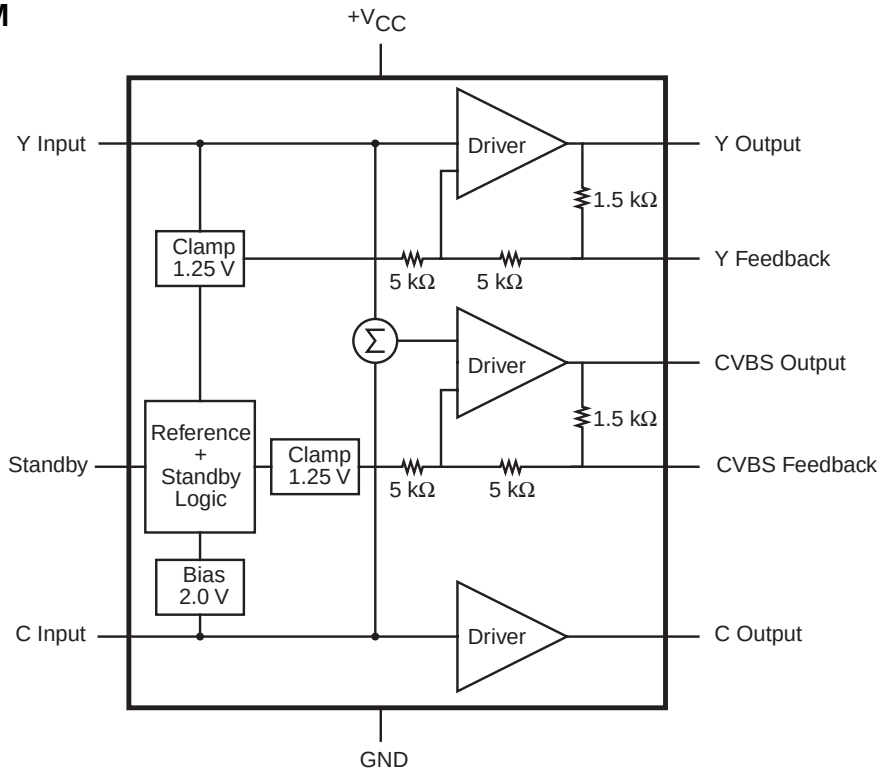
- Video Editing Equipment
- Video Capture/Playback Cards
- Video Tape Recorders
- TV Monitor Sources
- Multimedia PCs

GENERAL DESCRIPTION

The SPT9400 is a triple video line driver chip that takes standard Y/C analog inputs and provides simultaneous Y/C and composite video analog outputs for driving 75 Ω lines. Internal summing of the Y and C inputs is performed to produce composite video output. It is possible to achieve composite output on both the Y and CVBS outputs simultaneously by inputting a composite signal on the Y input. The luminance input is clamped at 1.25 V and amplified 6 dB to produce a 2 V_{P-P} (typical) into a series 75 Ω resistor and 75 Ω cable load. The internal 1.5 kΩ resistor provides gain compensation for low frequency signals. The chrominance input is biased at 2.0 V and amplified 6 dB to produce a 1.2 V_{P-P} (typical), into a series 75 Ω resistor and 75 Ω cable load.

The SPT9400 features a standby (active low) mode that draws only 113 µW of power. Nominal power dissipation (no input) is typically 168 mW. It requires a single +5 V supply, operates over the commercial temperature range (0 to +70 °C) and is available in a very small (5.0 x 4.4 mm) 12-lead Shrink Small Outline Package (SSOP).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{CC} ..... +6.0 V

Maximum Power Dissipation

P_D ..... 350 mW

Thermal Impedance (T_A=+25 °C and above)

Θ_{CA} ..... 2.8 mW/°C

Temperature

Operating Temperature ..... 0 to +70 °C

Storage Temperature ..... -55 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +5.0 V, V_{IN} = 1.0 V_{P-P} video signal, R_L = 150 Ω, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT9400 MIN	SPT9400 TYP	SPT9400 MAX	UNITS
Power Supply						
Supply Current (I_{CC})	No Input	I		33.5	45	mA
V_{CC} Voltage		IV	4.5	5.0	5.5	V
Power Dissipation		I		168	225	mW
Standby Current	Pin 5 Grounded	I		22.5	50	µA
Standby Power Dissipation	Pin 5 Grounded	I		113		µW
Digital Input						
Digital Input (Low)	Standby Pin 5	I	0.0	0.1	0.3	V
Digital Input (High)	Standby Pin 5	I	1.8	2.0	V_{CC}	V
Bias Voltages						
Clamp Voltage	Y Input Pin 2	I	1.05	1.25	1.45	V
Bias Voltage	C Input Pin 6	I	1.7	2.0	2.3	V
Dynamic Performance						
Voltage Gain		I	5.5	6.0	6.5	dB
Differential Gain	Ramp Input 3.58 MHz	I	-3.0	-1.5	+3.0	%
Differential Phase	Ramp Input 3.58 MHz	I	-3.0	+0.2	+3.0	Degrees
Frequency Response	f_{IN} = 1 to 5 MHz	V		0.0		dB
Cross Talk	Y_{IN} to C_{OUT}	V		-40		dB
	C_{IN} to Y_{OUT}	V		-40		dB

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Typical Interface Circuit

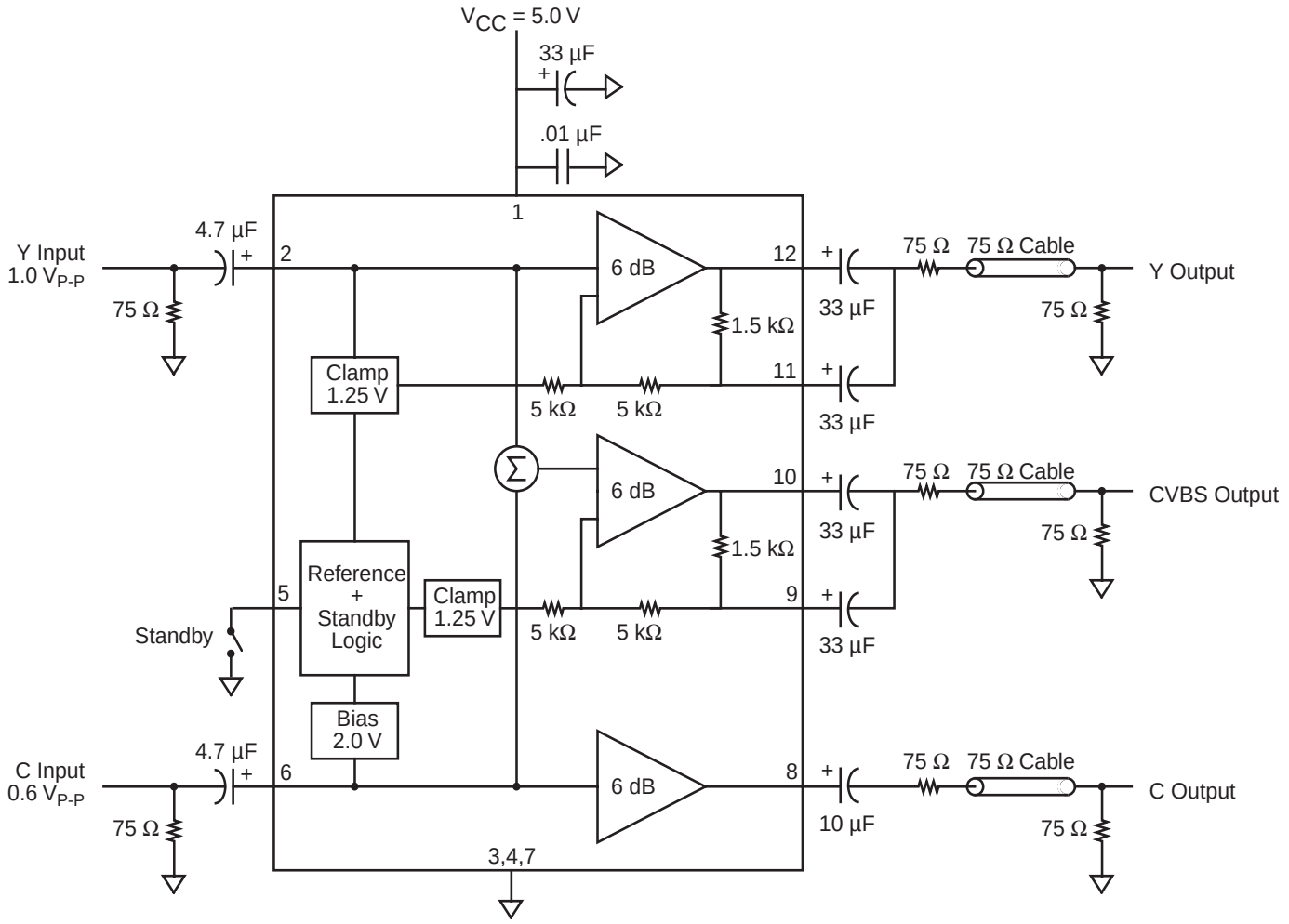


Figure 2 - CVBS Output (Multiburst Test)

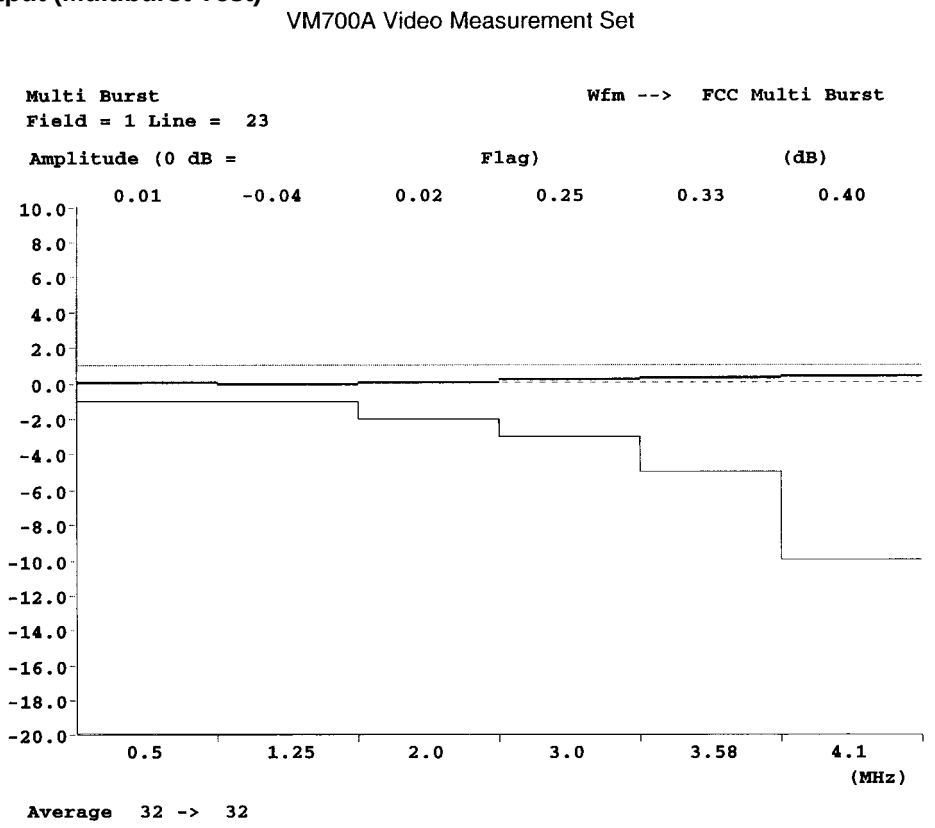


Figure 3 - CVBS Output (DP/DG)

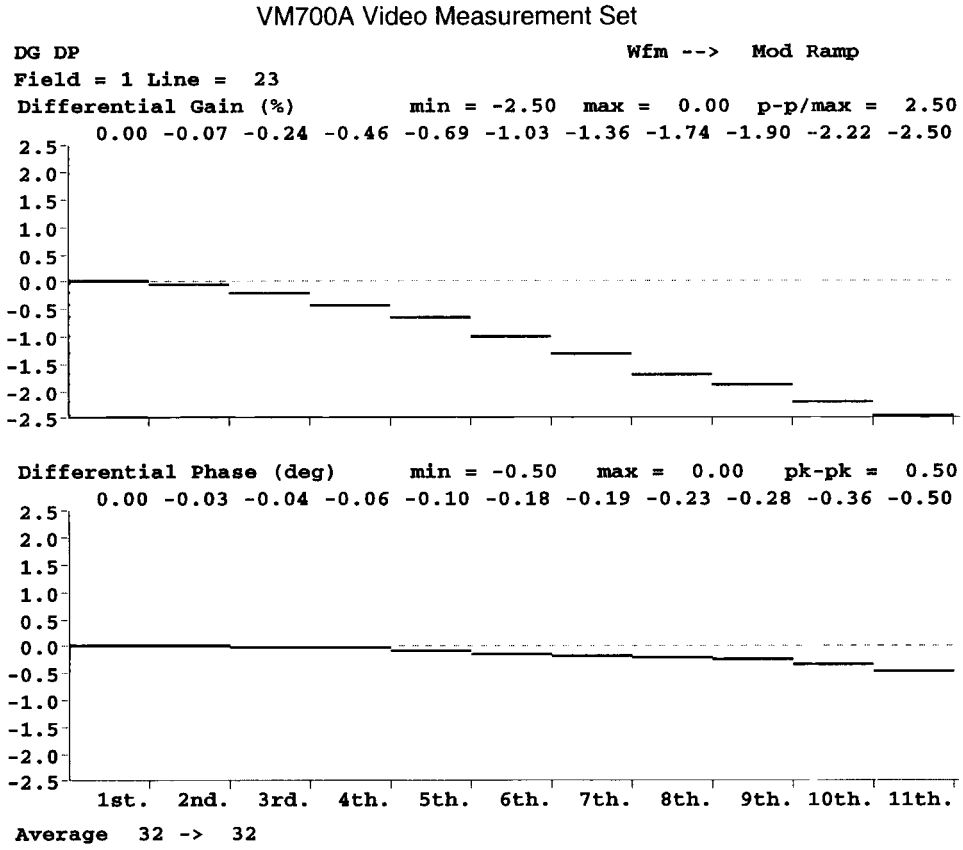


Figure 4 - CVBS Output (Vector Scope)

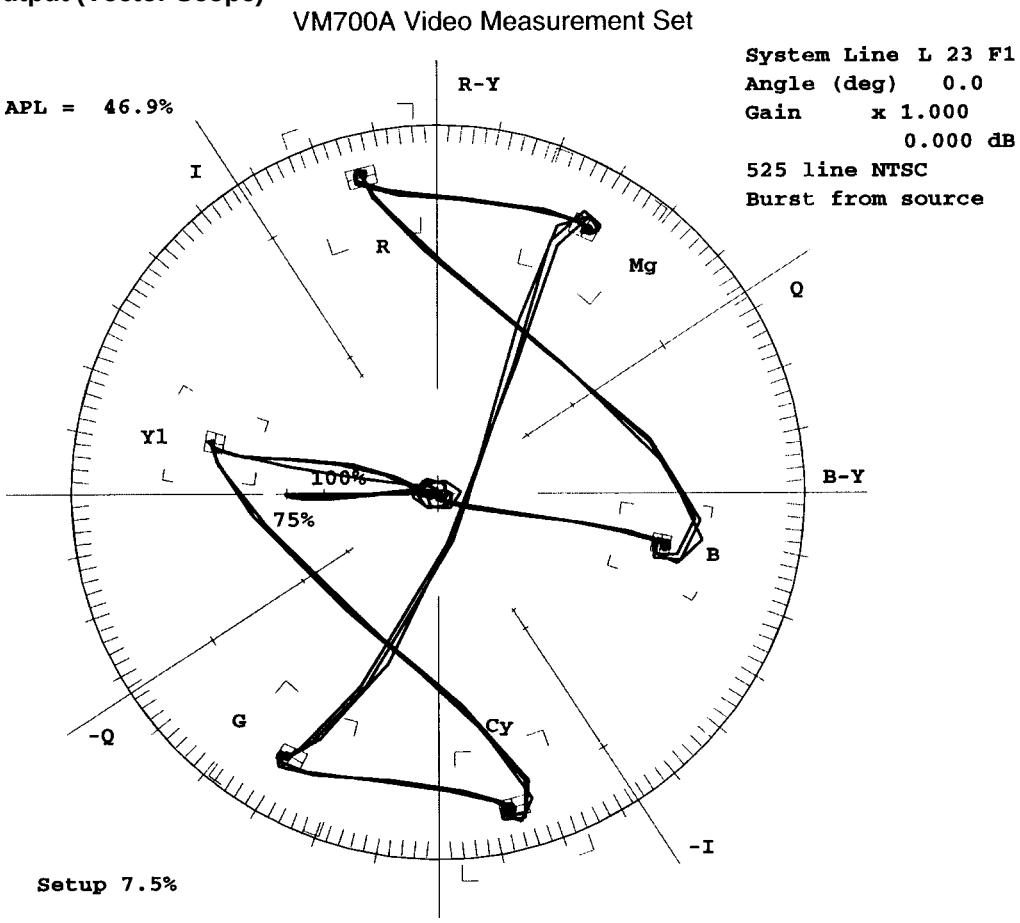
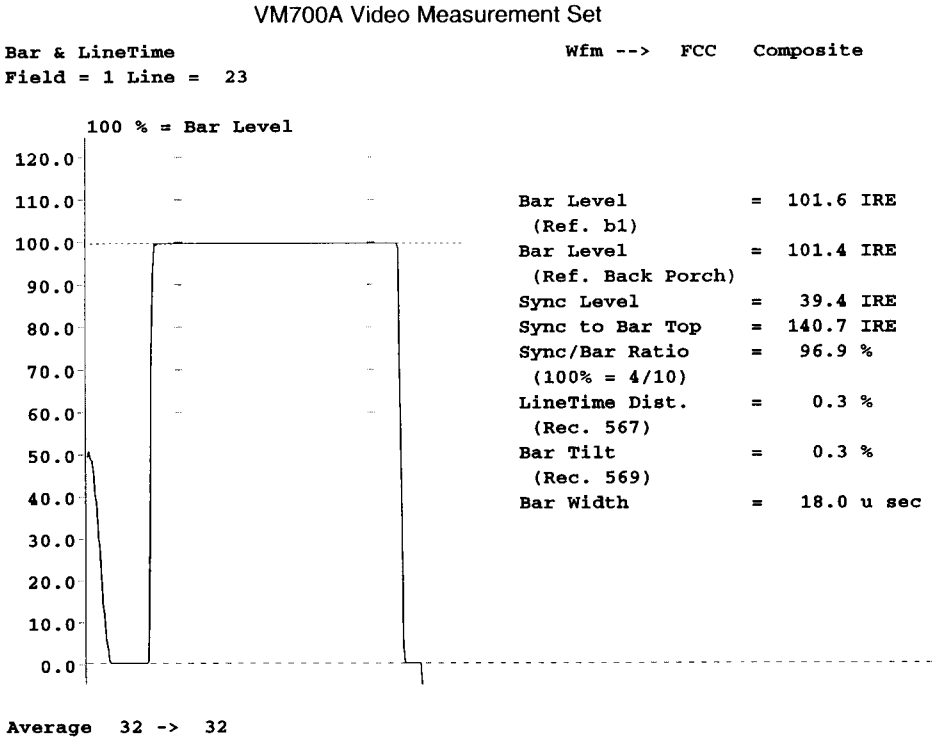
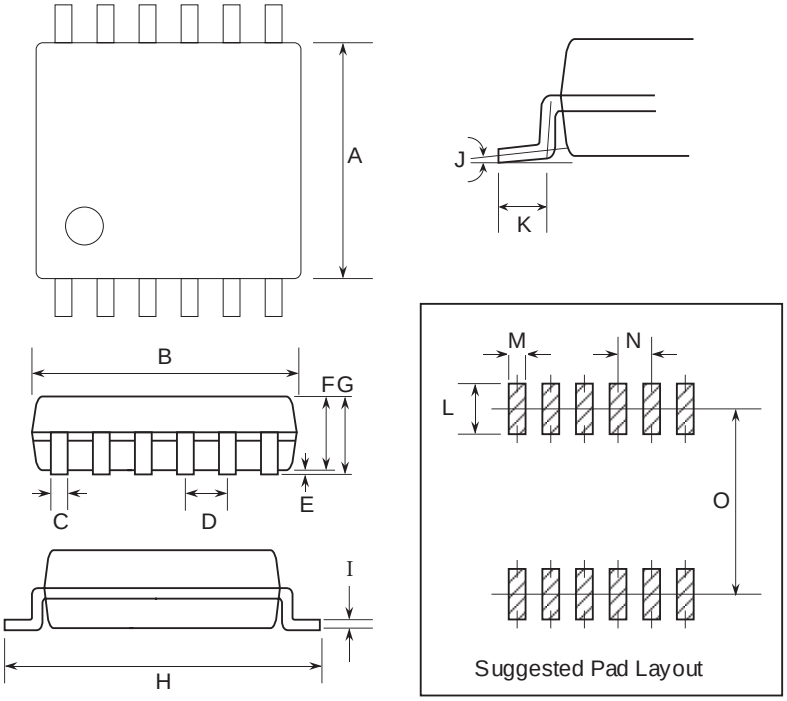


Figure 5 - CVBS Output (Bar and Line Time)



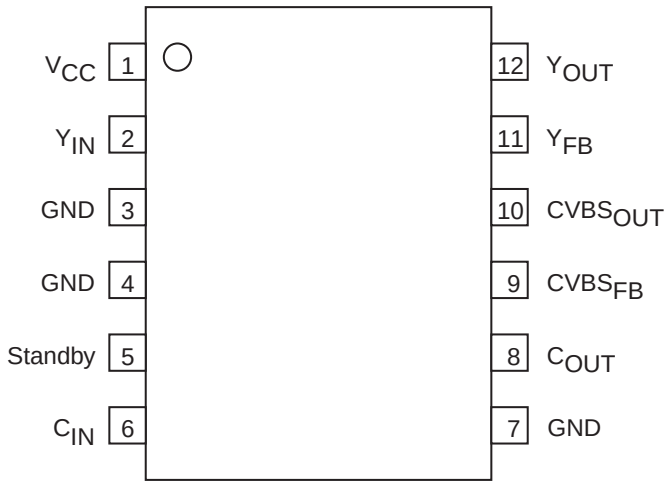
PACKAGE OUTLINE

12-Lead SSOP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.181	4.2	4.6
B	0.189	0.205	4.8	5.2
C	0.012 typ		0.3 typ	
D	0.031 typ		0.8 typ	
E	0.000	0.008	0.0	0.2
F	0.047	0.063	1.2	1.6
G		0.067 max		1.7 max
H	0.264	0.248	6.7	6.3
I	0.004	0.010	0.10	0.25
J	0-10°		0-10°	
K	0.012	0.028	0.3	0.7
L	0.047 typ		1.2 typ	
M	0.016 typ		0.4 typ	
N	0.031 typ		0.8 typ	
O	0.213 typ		5.4 typ	

PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
Y_{IN}	Luminance (Y) Signal Input (typically 1 V_{P-P}, AC coupled)
C_{IN}	Chrominance (C) Signal Input (typically 0.62 V_{P-P}, AC coupled)
Standby	Power Down Standby Mode Select (Low = Standby, Internal Pull-Up)
Y_{OUT}	Luminance (Y) Output (typically 2.0 V_{P-P}, R_L = 150 Ω, AC coupled)
Y_{FB}	Luminance Feedback Pin
$CVBS_{OUT}$	Composite Video (CVBS) Output (typically 2.0 V_{P-P}, R_L = 150 Ω, AC coupled)
$CVBS_{FB}$	Composite Video Feedback Pin
C_{OUT}	Chrominance (C) Output (typically 1.3 V_{P-P}, R_L = 150 Ω, AC coupled)
V_{CC}	+5.0 V Supply
GND	Ground

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT9400SCR	0 to +70°C	12-Lead SSOP

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.