FAIRCHILD
SEMICONDUCTOR®

SPT9110

100 MSPS SINGLE-TO-DIFFERENTIAL TRACK-AND-HOLD

FEATURES

- 400 MHz Sampling Bandwidth
- 100 MHz Sampling Rate
- Excellent Hold Mode Distortion
  - -66 dB @ 50 MSPS (f_{IN} = 25 MHz)
  - -58 dB @ 100 MSPS (f_{IN} = 50 MHz)
- Track Mode Slew Rate: 700 V/µs
- Low Power: 120 mW Differential Mode
  75 mW Single-Ended Mode
- Single +5 V Supply
- Internal +2.5 V Reference

APPLICATIONS

- THA for Differential ADCs
- RF Demodulation Systems
- Test Instrumentation
- Digital Sampling Oscilloscopes

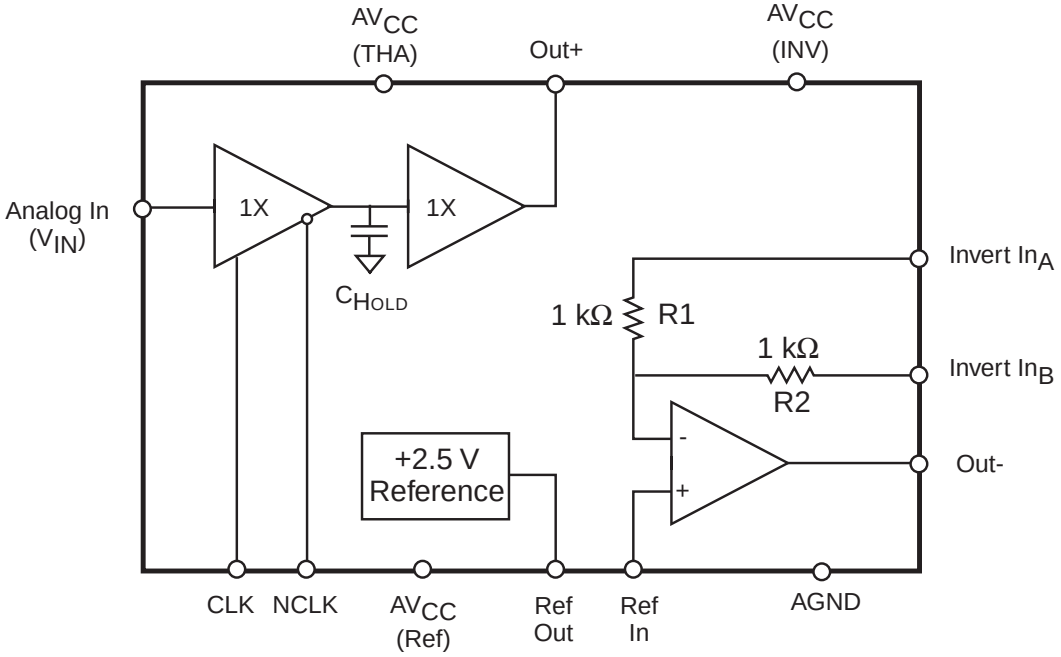
GENERAL DESCRIPTION

The SPT9110 is a single-to-differential track-and-hold amplifier. It can be operated as a single-end THA only or, in full configuration, as a single-to-differential THA. An internal reference provides the common-mode voltage for the single-to-differential output stage. The THA, inverter and reference have separate power supply pins so each can be optionally powered up and used.

This device provides an analog designer with a low cost single-to-differential THA amplifier for interfacing differential and single-ended ADCs.

The SPT9110 is offered in a 28-lead SOIC package in the industrial temperature range.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages

AV_{CC} Supplies ..... -0.5 to +6 V

Input Voltages

Analog Input Voltage ..... -0.5 to +6 V
CLK, NCLK Input ..... -0.5 to +6 V
Ref In ..... -0.5 to +6 V

Output Currents[2]

Continuous Output Current ..... ±15 mA

Temperature

Operating Temperature ..... -40 to +85 °C
Junction Temperature ..... +150 °C
Lead, Soldering (10 seconds) ..... +220 °C
Storage ..... -65 to +150 °C

Note 1: Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical application.
Note 2: Outputs are short circuit protected.

ELECTRICAL SPECIFICATIONS

AV_{CC} = +5.0 V, AGND = 0.0 V, Output Load = 1 kΩ and 10 pF, V_{IN} = 2.0 Vp-p,Internal Reference, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT9110 MIN	SPT9110 TYP	SPT9110 MAX	UNITS
DC Performance						
Gain ΔV_{IN} = 2.0 Vp-p						
Single Ended Out	+25 °C	I	0.95	0.97	0.99	V/V
	Full Temperature	V		0.96		V/V
Differential Out	+25 °C	I	1.80	1.93	2.00	V/V
	Full Temperature	V		1.92		V/V
Offset V_{IN} = +2.5 V						
Out+	+25 °C	I	-100	±50	+100	mV
	Full Temperature	V		55		mV
Differential[1]	+25 °C, Ref In=Out+ CM	I	-15	±5	±15	mV
	Full Temperature	V		10		mV
Output Drive Capacity[2]	Full Temperature	IV		±1	±10	mA
Output Load at 10 pF	Full Temperature	V		1		kΩ
Analog Input/Output						
Output Voltage Range	Full Temperature	VI	1.5		3.5	V
Input Capacitance	+25 °C	V		5		pF
Input Resistance	+25 °C	I	100	140		kΩ
Reference Voltage Output		I	2.35	2.45	2.55	V
Reference Output Current[3]	+25 °C	V		±100		µA
Reference Voltage Tempco	Full Temperature	V		75		ppm/°C
Clock Inputs						
Input Type/Logic Family		V		Differential PECL		
Input Bias Current	+25 °C	I		2	10	µA
Input Low Voltage (Differential)	+25 °C	I		3.3	3.5	V
Input High Voltage (differential)	+25 °C	I	3.9	4.1		V

[1]Differential offset is specified with Ref In equal to the common mode output voltage of OUT+ and so includes the offset error of the inverter only.
[2]This part is intended to drive a high impedance load. AC performance is degraded at ±10 mA. See the Typical Performance Graphs.
[3]Ref Out has a typical output impedance of 1 kΩ and should be buffered for driving loads other than Ref In.

ELECTRICAL SPECIFICATIONS

AV_{CC} = +5.0 V, AGND = 0.0 V, Output Load = 1 kΩ and 10 pF, V_{IN} = 2.0 Vp-p,Internal Reference, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT9110 MIN	SPT9110 TYP	SPT9110 MAX	UNITS
Track Mode Dynamics						
Bandwidth (-3 dB)	+25 °C					
Single Ended Out		V		220		MHz
Differential Out		V		140		MHz
Slew Rate 2.0 Vp-p Output Step	+25 °C					
Single Ended Out	20 pF Load	IV		580		V/µs
Differential Out[7]	20 pF Load	IV		800		V/µs
Input RMS Spectral Noise	Single Ended	V		3.5		$nV/\sqrt{Hz}$
	Differential	V		13.0		$nV/\sqrt{Hz}$
Track-to-Hold Switching						
Aperture Delay	+25 °C	V		250		ps
Aperture Jitter	+25 °C	V		<1		ps rms
Pedestal Offset	+25 °C	IV		±12		mV
	Full Temperature	V		±12		mV
Hold Mode Dynamics[4] (V_{IN} = 1 Vp-p)						
Worst Harmonic						
5 MHz, 50 MSPS, Single-Ended	T_A = +25 °C	IV	-64	-68		dB
	T_A = -40 °C to +85 °C	V		-64		dB
Worst Harmonic						
5 MHz, 50 MSPS, Differential	T_A = +25 °C	IV	-61	-65		dB
	T_A = -40 °C to +85 °C	V		-63		dB
Worst Harmonic						
25 MHz, 50 MSPS, Single-Ended	T_A = +25 °C	V		-66		dB
	T_A = -40 °C to +85 °C	V		-63		dB
Worst Harmonic						
25 MHz, 50 MSPS, Differential	T_A = +25 °C	V		-64		dB
	T_A = -40 °C to +85 °C	V		-60		dB
Worst Harmonic						
50 MHz, 100 MSPS, Single-Ended	T_A = +25 °C	IV	-54	-58		dB
	T_A = -40 °C to +85 °C	V		-54		dB
Worst Harmonic						
50 MHz, 100 MSPS, Differential	T_A = +25 °C	IV	-50	-54		dB
	T_A = -40 °C to +85 °C	V		-50		dB
Sampling Bandwidth[5] (-3 dB) V_{IN} = 2.0 Vp-p	+25 °C	V		400		MHz
Hold Noise[6] (RMS)	+25 °C	V		300 x t_H		mV/s
Droop Rate, V_{IN} = +2.5 V	+25 °C	IV		±40		mV/µs
	Full Temperature	IV		±80		mV/µs
Feedthrough Rejection (50 MHz) V_{IN}= 2 Vp-p	Full Temperature	V		-65		dB

4. For hold times longer than 50 ns, the input common mode voltage may affect the hold mode distortion. (This is due to nonlinear droop that varies with VCM.) For optimal performance, Fairchild recommends that the held output signal be used within 50 ns of the application of the hold signal.
5. Sampling bandwidth is defined as the -3 dB frequency response of the input sampler to the hold capacitor when operating in the sampling mode. It is greater than tracking bandwidth because it does not include the bandwidth of the output amplifier.
6. Hold mode noise is proportional to the length of time a signal is held. This value must be combined with the track mode noise to obtain total noise.
7. Optimized for hold mode performance and low power.

ELECTRICAL SPECIFICATIONS

AV_{CC} = +5.0 V, AGND = 0.0 V, R_{Load} = 1 kΩ and 10 pF, V_{IN} = 2.0 Vp-p, Internal Reference, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT9110 MIN	SPT9110 TYP	SPT9110 MAX	UNITS
Hold-to-Track Switching[8]						
Acquisition Time to 0.1%	+25 °C	V		3.5		ns
1 V Output Step						
Acquisition Time to 0.025%	+25 °C	V		4.0		ns
1 V Output Step						
Power Supplies						
Supply Voltage		IV	4.75	5	5.25	V
Supply Current						
Single Ended Output Mode[9]		I		15	20	mA
Differential Output Mode		I		24	30	mA
Power Dissipation						
Single Ended Output Mode[9]		I		75	100	mW
Differential Output Mode		I		120	150	mW
Power Supply Rejection Ratio	+25 °C	V		44		dB
Single-Ended Output	ΔV_{CC} = 0.5 V_{P-P}					

8. Measured at the hold capacitor.
9. Inverter powered down.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

TIMING SPECIFICATION DEFINITIONS

ACQUISITION TIME

This is the time it takes the SPT9110 to acquire the analog signal at the internal hold capacitor when it makes a transition from hold mode to track mode. (See figure 1.) The acquisition time is measured from the 50% input clock transition point to the point when the signal is within a specified error band at the internal hold capacitor (ahead of the output amplifier). It does not include the delay and settling time of the output amplifier. Because the signal is internally acquired and settled at the hold capacitor before the output voltage has settled, the sampler can be put in hold mode before the output has settled.

TRACK-TO-HOLD SETTLING TIME

The time required for the output to settle to within 4 mV of its final value.

APERTURE DELAY

The aperture delay time is the interval between the leading edge transition of the clock input and the instant when the input signal was equal to the held value. It is the difference in time between the digital hold switch delay and the analog signal propagation time.

Figure 1 - Timing Diagram

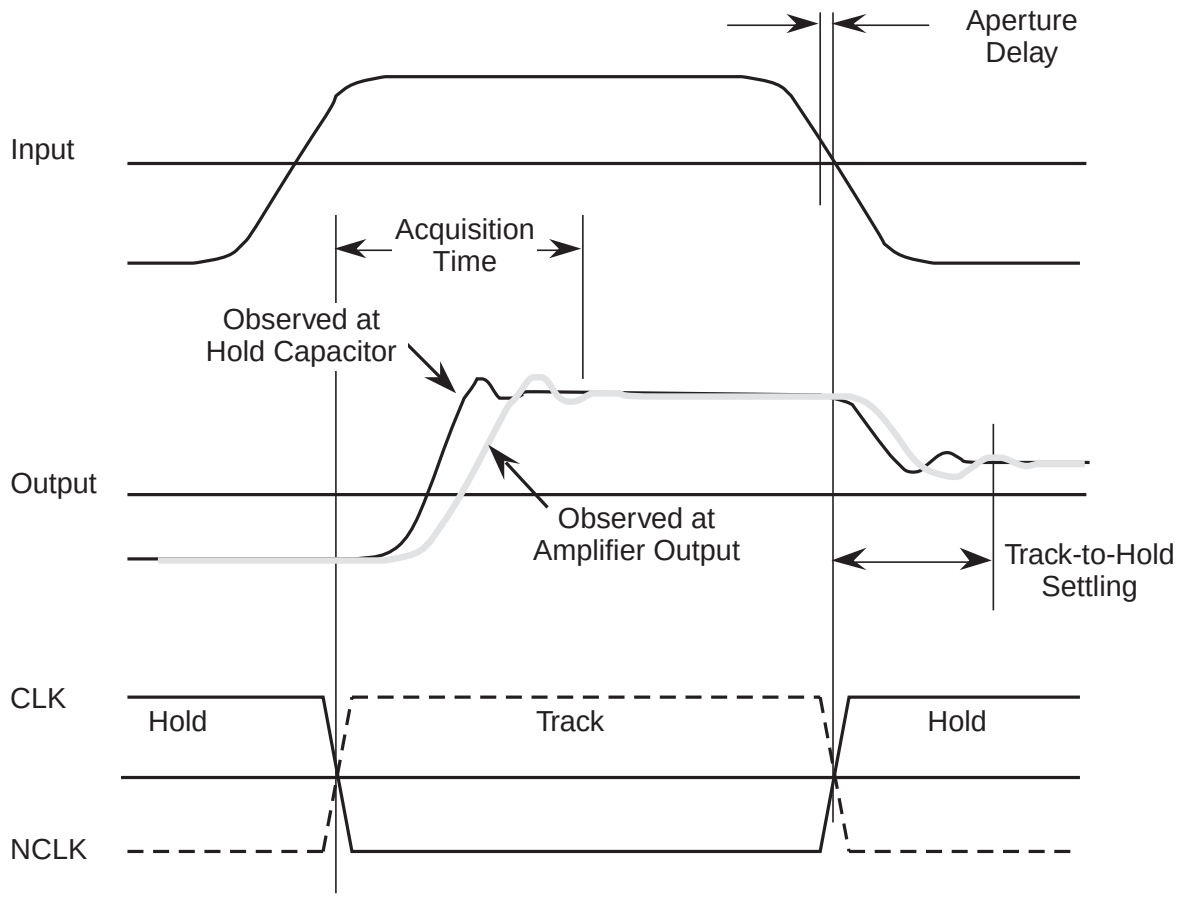
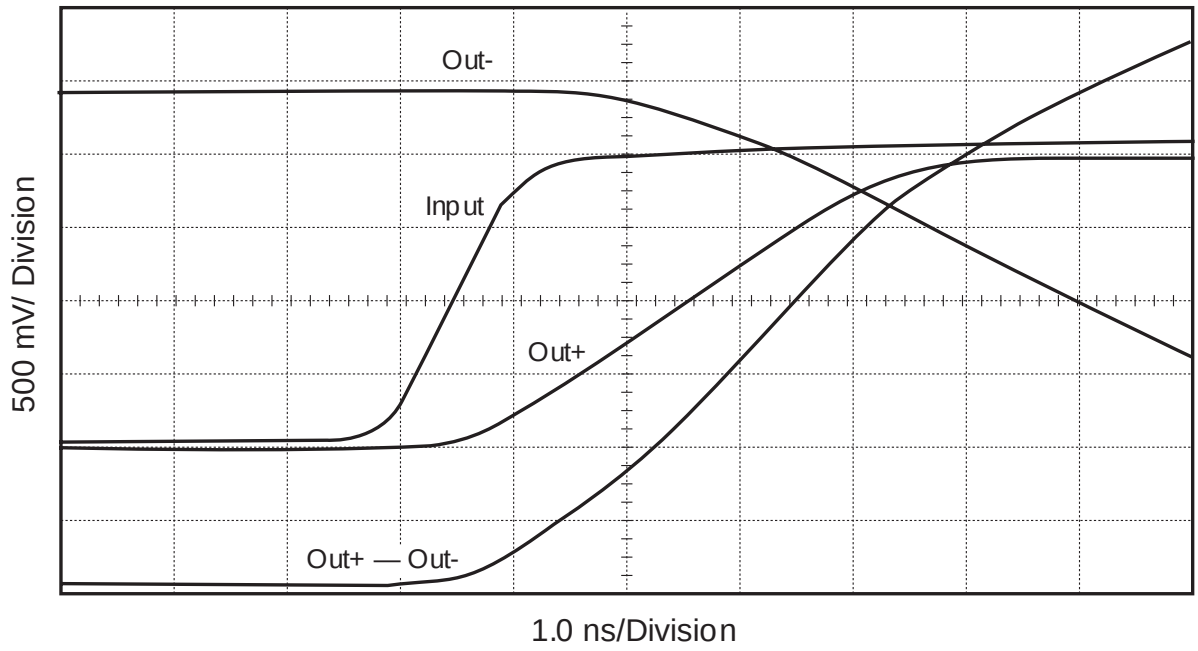


Figure 2 - Typical Output Response to Step Input



GENERAL DESCRIPTION

The SPT9110 is a low cost 100 MSPS track-and-hold amplifier with single ended (75 mW) or differential output (120 mW). It consists of three components. The first is a single-ended track-and-hold amplifier (THA) with a 1.5 to 3.5 V input range and PECL clock inputs. The second is an inverting op amp with gain of -1 to provide the differential output (OUT-). The third component is a 2.5 V bandgap reference for the inverter.

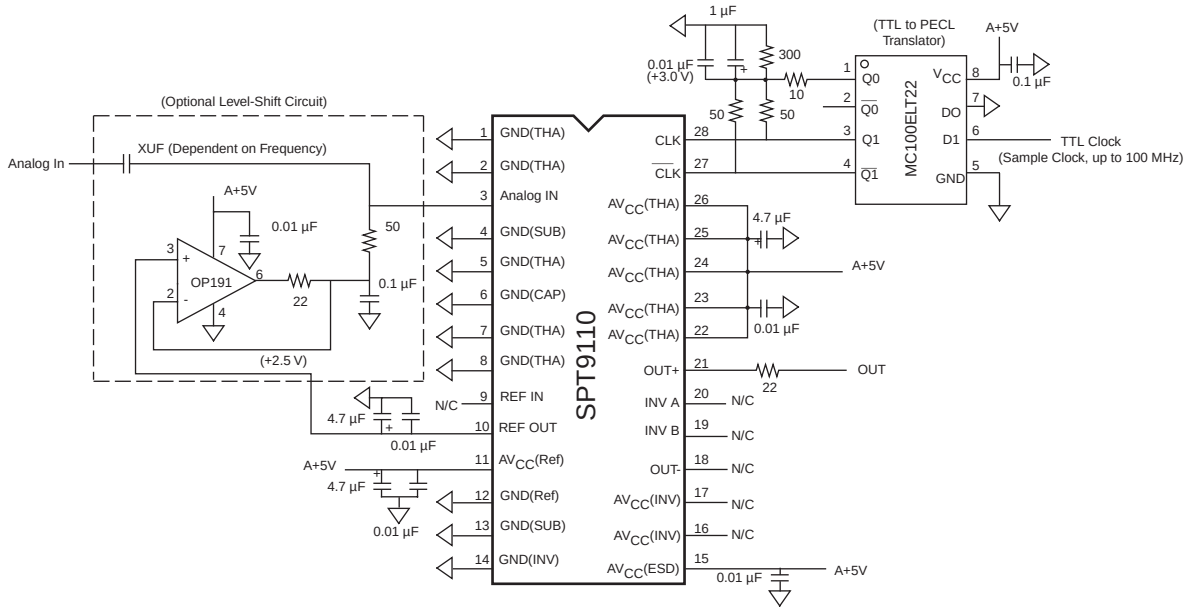
PARTITIONED POWER SUPPLY MANAGEMENT

Three separate +5 V supply connections power the THA, inverting the op amp and bandgap reference. Unused components can be powered off to minimize power dissipation.

The single-ended mode requires use of only the THA and output on the OUT+ pin. In this mode the reference and inverter may be powered down.

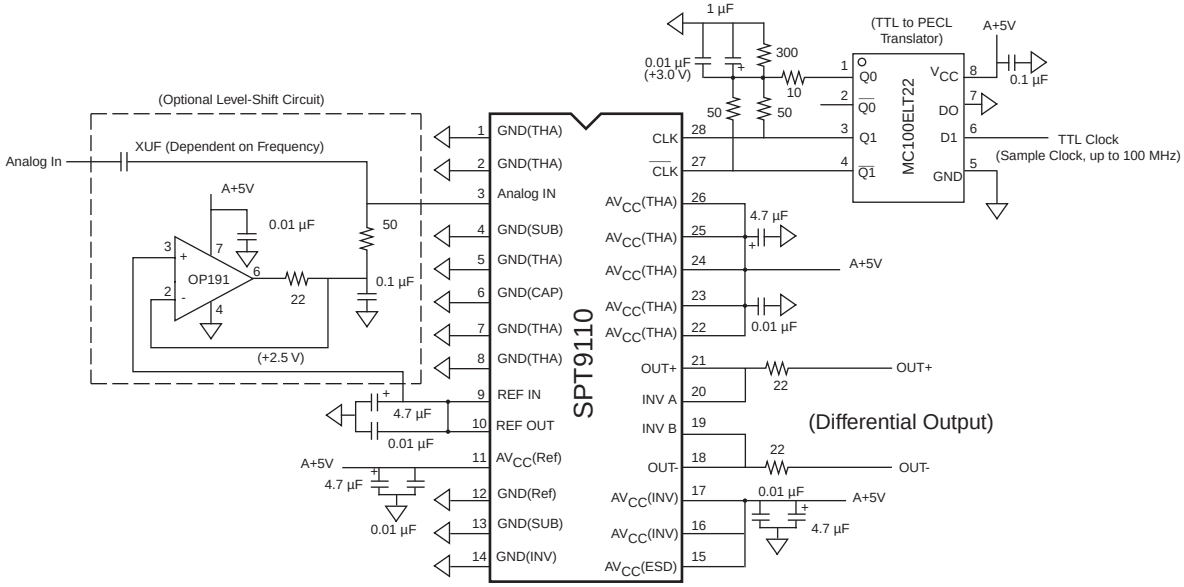
The differential mode requires use of all three components (unless an external reference is supplied). The output is measured between OUT+ and OUT- in this mode.

Figure 3 - Typical Interface Circuit (Single-Ended Operational Design)



Notes:
1. Input signal is typically at a +2.5 V offset. The optional level-shift circuit may be eliminated if driving from a source that already provides for this offset.
2. The device may be operated from -5 V supply on GND pins and 0 V on AV_{CC} pins. All input and output pins will be shifted by -5 V. The use of an ECL level may be used to drive the clock inputs.
3. V_{CC} (ESD) is the high voltage for the ESD protection diodes and must be connected in all applications. NOTE: It should be tied to V_{CC} (THA), not to V_{CC} (INV).

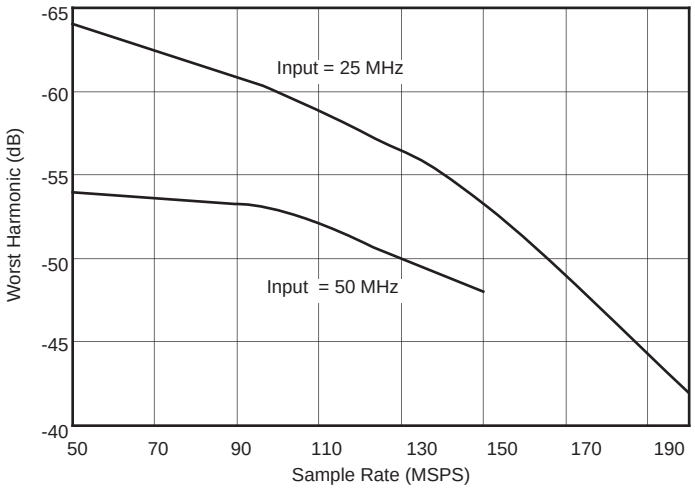
Figure 4 - Typical Interface Circuit (Differential Operational Design)



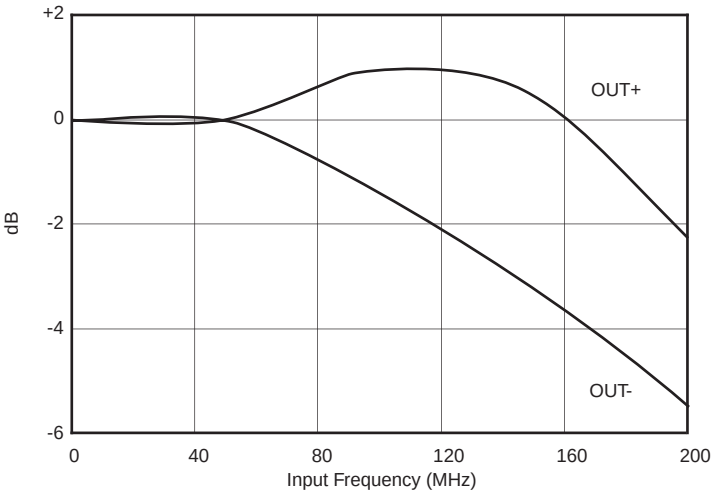
Notes:
1. Input signal is typically at a +2.5 V offset. The optional level-shift circuit may be eliminated if driving from a source that already provides for this offset.
2. The device may be operated from -5 V supply on GND pins and 0 V on AV_{CC} pins. All input and output pins will be shifted by -5 V. The use of an ECL level may be used to drive the clock inputs.
3. V_{CC} (ESD) is the high voltage for the ESD protection diodes and must be connected in all applications. NOTE: It should be tied to V_{CC} (THA), not to V_{CC} (INV).

TYPICAL PERFORMANCE CHARACTERISTICS

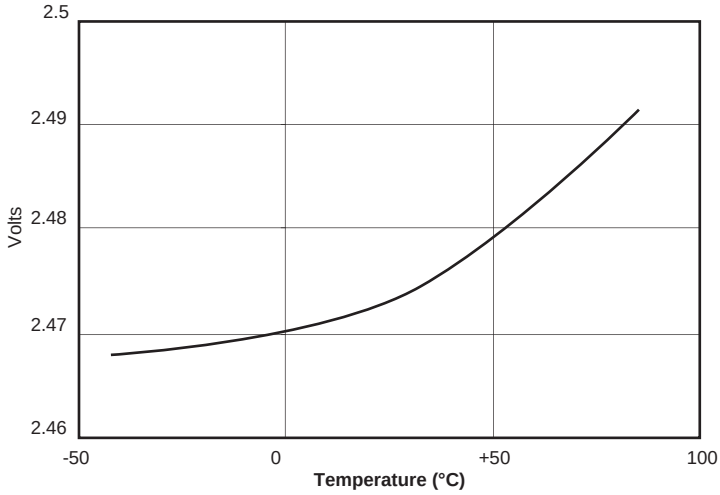
Single-Ended (OUT+) Hold Mode Distortion vs. Sample Rate



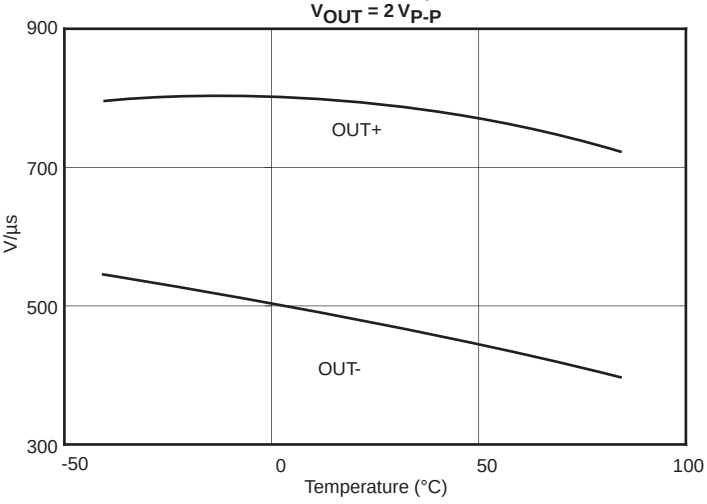
Track Mode Bandwidth



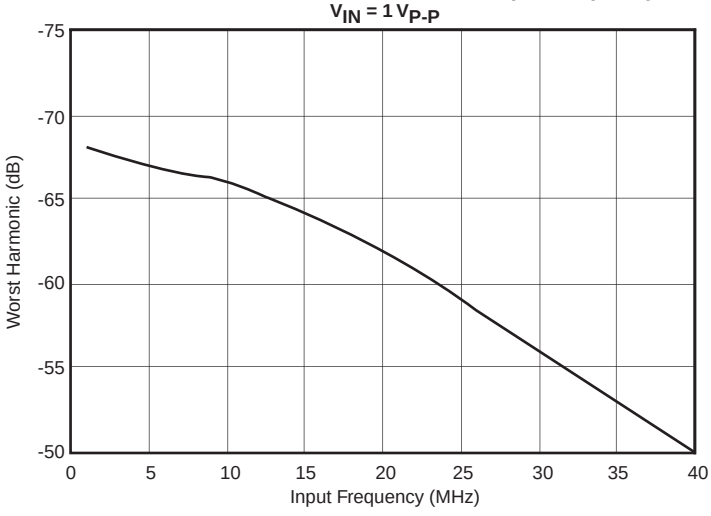
Reference Output Voltage vs. Temperature



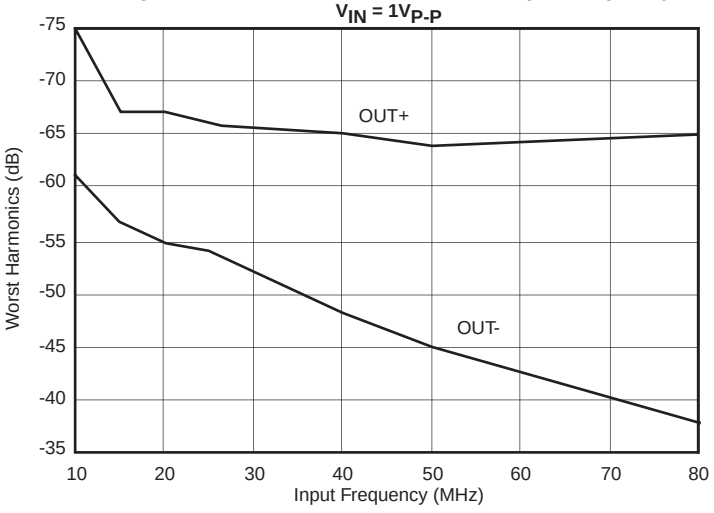
Slew Rate vs. Temperature
V_{OUT} = 2 V_{P-P}



Differential Track Mode Distortion vs. Input Frequency
V_{IN} = 1 V_{P-P}

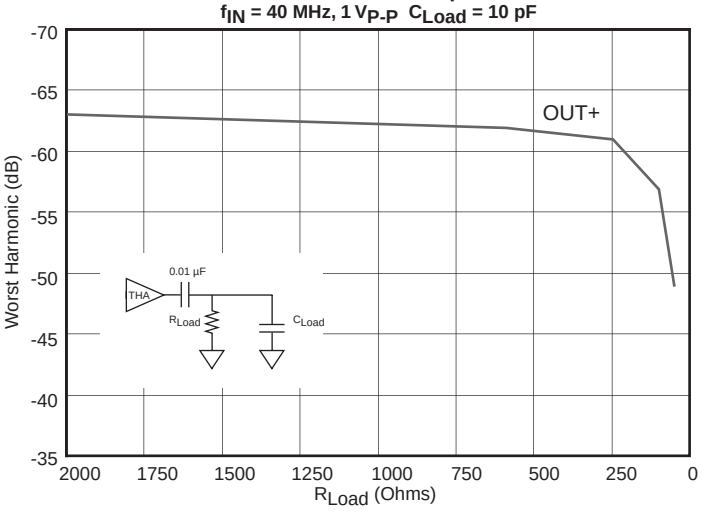


Single Ended Track Mode Distortion vs. Input Frequency
V_{IN} = 1V_{P-P}

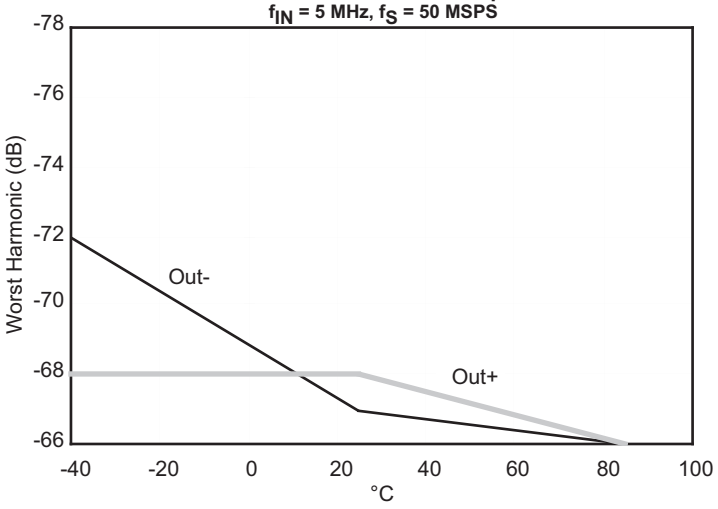


TYPICAL PERFORMANCE CHARACTERISTICS

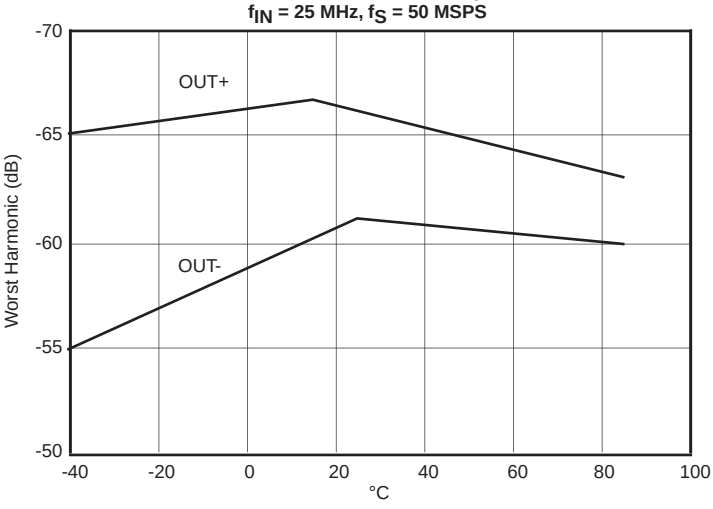
Track Mode Distortion vs. AC Coupled Resistive Load
f_{IN} = 40 MHz, 1 V_{P-P} C_{Load} = 10 pF



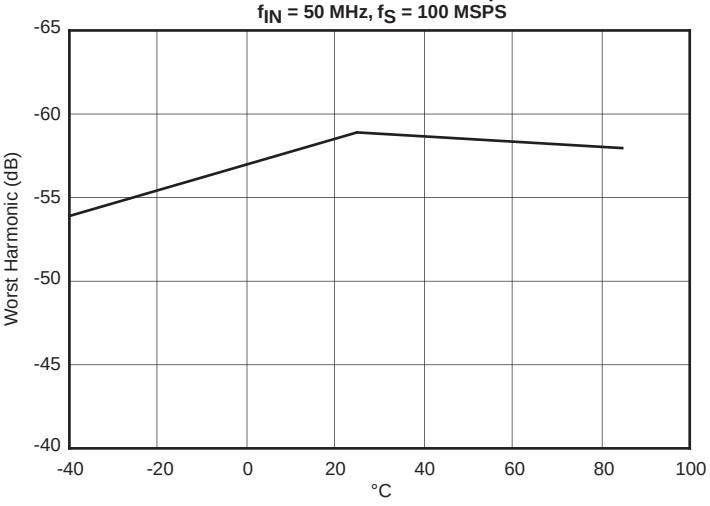
Hold Mode Distortion vs. Temperature
f_{IN} = 5 MHz, f_S = 50 MSPS



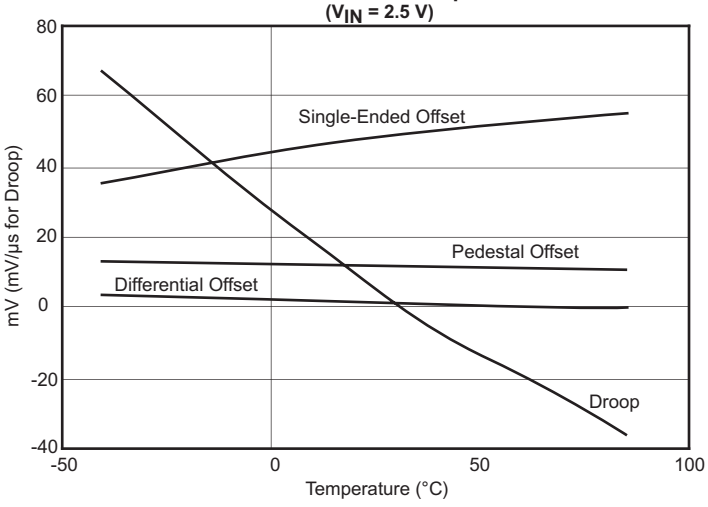
Hold Mode Distortion vs. Temperature
f_{IN} = 25 MHz, f_S = 50 MSPS



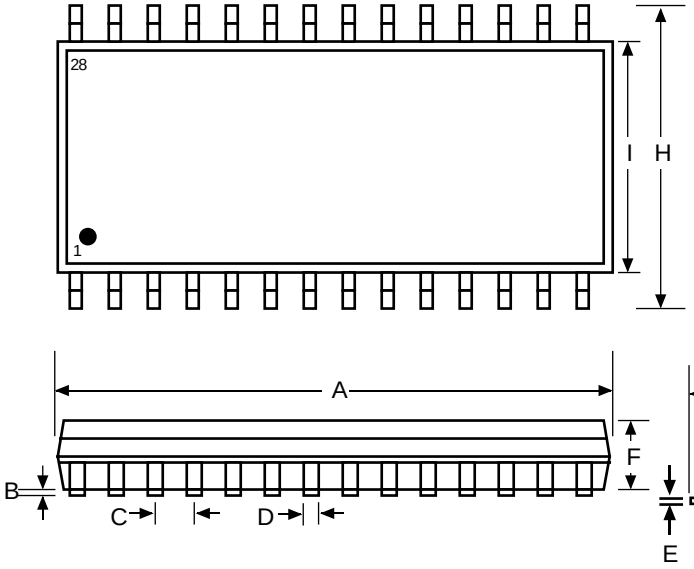
Hold Mode Distortion vs. Temperature
f_{IN} = 50 MHz, f_S = 100 MSPS



DC Parameters vs. Temperature
(V_{IN} = 2.5 V)

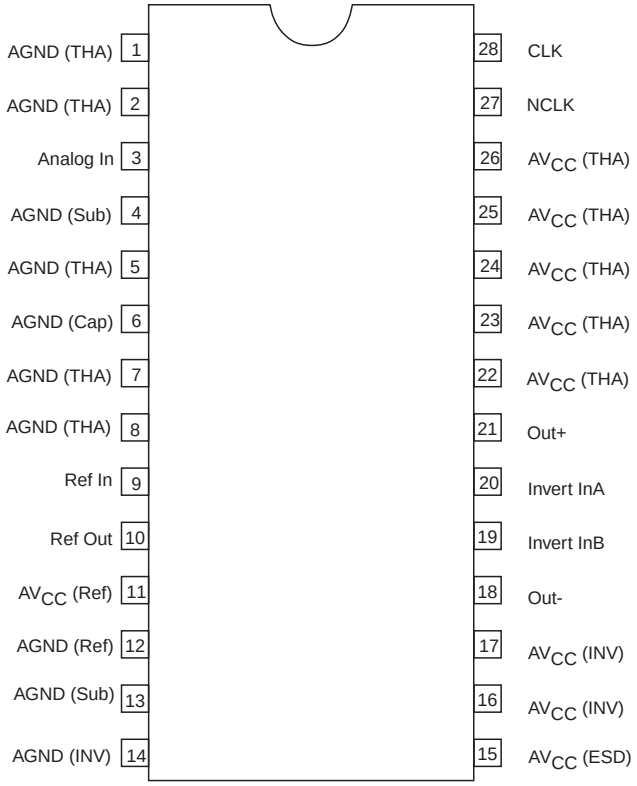


PACKAGE OUTLINE
28-LEAD SOIC



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.696	0.712	17.68	18.08
B	0.004	0.012	0.10	0.30
C		.050 typ	0.00	1.27
D	0.014	0.019	0.36	0.48
E	0.009	0.012	0.23	0.30
F	0.080	0.100	2.03	2.54
G	0.016	0.050	0.41	1.27
H	0.394	0.419	10.01	10.64
I	0.291	0.299	7.39	7.59

PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
Analog In	Single-ended analog input to the THA
Invert InA	Inverting input A to inverting amplifier resistor R1
Invert InB	Inverting input B to inverting amplifier resistor R2
Out+	Single-ended output of the THA
Out-	Output from the inverting amplifier
CLK	Noninverting differential PECL clock input
NCLK	Inverting differential PECL clock input
Ref In	Common-mode reference for the inverting amplifier
Ref Out	Internal +2.5 V reference output
AV_{CC} (THA)	Track-and-hold analog +5 V supply
AV_{CC} (INV)	Inverter +5 V supply
AV_{CC} (Ref)	Internal reference +5 V supply
AV_{CC} (ESD)	+5 V supply for ESD protection diodes
AGND (THA)	Track-and-hold analog ground
AGND (Cap)	Hold capacitor analog ground
AGND (Sub)	Substrate analog ground
AGND (INV)	INVERTER analog ground
AGND (Ref)	Internal reference analog ground

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT9110SIS	-40 to +85 °C	28L SOIC

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.