FAIRCHILD
SEMICONDUCTOR®

SPT7864

10-BIT, 40 MSPS A/D CONVERTER

TECHNICAL DATA

NOVEMBER 20, 2001

FEATURES

- 40 MSPS maximum sample rate
- 9.5 effective number of bits at f_{IN} = 10 MHz and f_S = 40 MSPS
- 2 V_{P-P} full-scale input range
- Differential input 2.5 V common mode
- Internal or external voltage reference
- Common-mode voltage reference output
- +3 V / +5 V digital output logic compatibility
- +5 V analog power supply
- Sleep mode power dissipation: 55 mW

APPLICATIONS

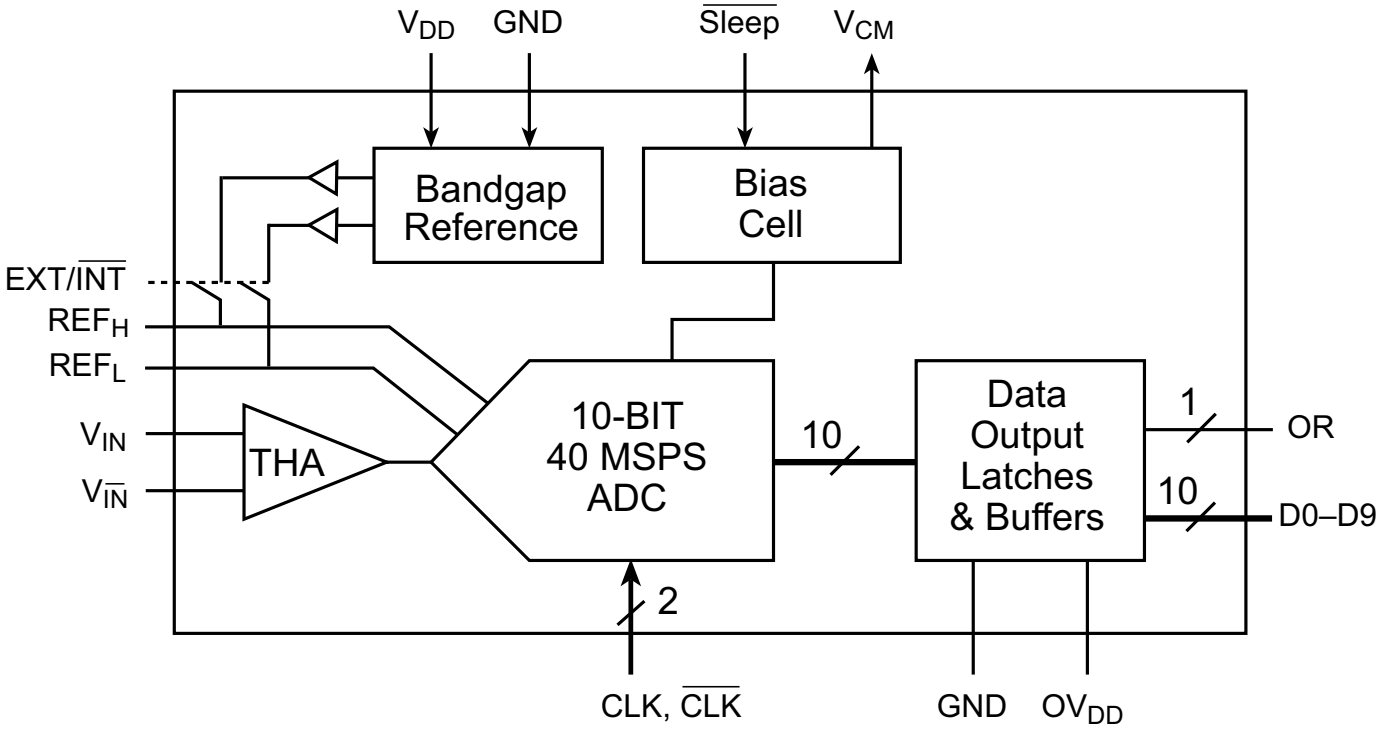
- Video imaging
- Medical imaging
- Radar receivers
- IR imaging
- Digital communications

GENERAL DESCRIPTION

The SPT7864 is a 10-bit, 40 MSPS analog-to-digital converter with low power dissipation at only 395 mW typical at 40 MSPS with a power supply of +5.0 V. The digital outputs are +3 V or +5 V, and are user selectable. The SPT7864 has incorporated proprietary circuit design and CMOS processing technologies to achieve its advanced performance. Inputs and outputs are TTL/CMOS compatible to interface with TTL/CMOS logic systems. Output data format is offset binary.

The SPT7864 is available in a 28-lead SSOP package over the commercial temperature range.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur) 25 °C

Supply Voltages

V_{DD} ..... 6.0 V
OV_{DD} ..... 6.0 V

Input Voltages

Analog Input ..... –0.3 V to V_{DD} +0.7 V
CLK Input ..... –0.3 V to V_{DD} +0.7 V

Output

Digital Outputs ..... –0.3 V to V_{DD} +0.7 V

Temperature

Operating Temperature ..... 0 to +70 °C
Storage Temperature ..... –65 to +150 °C

Note: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{DD}=+5.0 V, f_S=40 MSPS, V_{REFH}=3.0 V, V_{REFL}=2.0 V, OV_{DD}=3.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7864 MIN	SPT7864 TYP	SPT7864 MAX	UNITS
Resolution			10			Bits
DC Accuracy						
Differential Linearity Error (DLE)	@ +25 °C	V		±0.5		LSB
	full temperature	V		±0.75		LSB
Integral Linearity Error (ILE)	@ +25 °C	V		±0.6		LSB
	full temperature	V		±1.0		LSB
No Missing Codes		VI		Guaranteed		
Analog Input						
Input Voltage Range (Differential)		V		±1		V
Input Common Mode (V_{CM})		IV	2	2.5	3	V
Input Capacitance		V		2		pF
Input Bandwidth		V	98			MHz
Common Mode Rejection Ratio (CMRR)		V		50		dB
Timing Characteristics						
Conversion Rate		VI			40	MSPS
Pipeline Delay (Latency)		IV		6		clocks
Output Delay (t_D)		V		7.5		ns
Aperture Delay Time (t_{AP})		V		1.5		ns
Aperture Jitter Time		V		15		ps (rms)
Dynamic Performance						
Effective Number of Bits (ENOB)						
f_{IN} = 10 MHz, f_{CLK} = 40 MSPS	25 °C	I	9.3	9.5		Bits
	0 °C to +70 °C	IV	9.3	9.5		Bits
Signal-to-Noise Ratio (SNR)						
f_{IN} = 10 MHz, f_{CLK} = 40 MSPS	25 °C	I	58	59		dB
	0 °C to +70 °C	IV	57	59		dB
Total Harmonic Distortion (THD)						
f_{IN} = 10 MHz, f_{CLK} = 40 MSPS	25 °C	I		–71	–66	dB
	0 °C to +70 °C	IV		–71	–65	dB
Signal-to-Noise and Distortion (SINAD)						
f_{IN} = 10 MHz, f_{CLK} = 40 MSPS	25 °C	I	57	59		dB
	0 °C to +70 °C	IV	57	59		dB
Spurious Free Dynamic Range (SFDR)						
f_{IN} = 10 MHz, f_{CLK} = 40 MSPS	25 °C	I	70	73		dB
	0 °C to +70 °C	IV	68	71		dB

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{DD}=+5.0 V, f_S=40 MSPS, V_{REFH}=3.0 V, V_{REFL}=2.0 V, OV_{DD}=3.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7864 MIN	SPT7864 TYP	SPT7864 MAX	UNITS
Power Supply Requirements						
V_{DD} Voltage (Analog Supply)		IV	4.75	5.0	5.25	V
OV_{DD} Voltage (Output Supply)		IV	2.7	3.0/5.0	5.25	V
V_{DD} Current		VI		74		mA
OV_{DD} Current		VI		8		mA
Power Dissipation						
External Voltage Reference		VI		387	417	mW
Internal Voltage Reference		VI		395	425	mW
Sleep Mode Power Dissipation						
External Voltage Reference		VI		45	47	mW
Internal Voltage Reference		VI		55	56	mW
Power Supply Rejection Ratio (PSRR)		V		45		dB
Internal References						
Common Mode Voltage Reference (V_{CM})	IO = –1 µA	VI	2.4	2.5	2.6	V
Common Mode Voltage Tempco		V		100		ppm/°C
Output Impedance (V_{CM})		V		2		kΩ
Reference Low Output Voltage (V_{REFL})	(EXT/$\overline{INT}$) = 0	VI	1.95	2.0	2.05	V
Reference High Output Voltage (V_{REFH})	(EXT/$\overline{INT}$) = 0	VI	2.95	3.0	3.05	V
External References						
Reference Low Input Voltage Range	(EXT/$\overline{INT}$) = 1	IV	1.7	2.0	2.3	V
Reference High Input Voltage Range	(EXT/$\overline{INT}$) = 1	IV	2.7	3.0	3.3	V
Digital Outputs						
Output Voltage High	IO = –2 mA	VI	85% OV_{DD}	90% OV_{DD}	OV_{DD}	V
Output Voltage Low	IO = 2 mA	VI		0.2	0.4	V
Digital Inputs						
Input High Voltage		VI	80% V_{DD}			V
Input Low Voltage		VI			20% V_{DD}	V
Input High Current		VI			±100	µA
Input Low Current		VI			±100	µA
Clock Inputs						
Clock Inputs High Voltage		VI	2		5	V
Clock Inputs Low Voltage		VI			0.4	V
Clock Inputs High Current		VI			±115	µA
Clock Inputs Low Current		VI			±115	µA

TEST LEVEL CODES

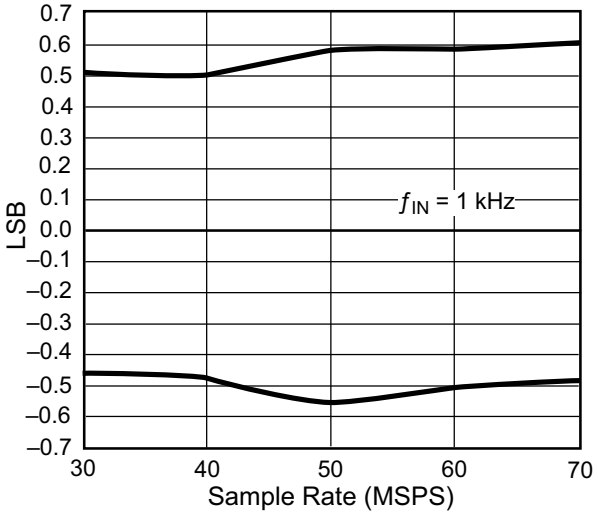
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

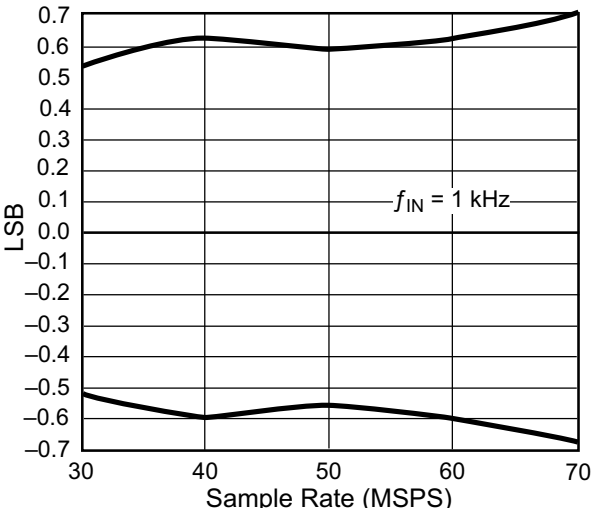
TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

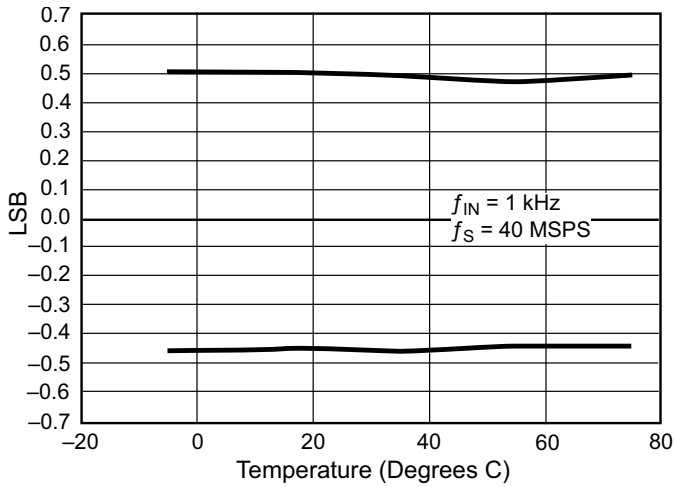
DLE Versus Sample Rate



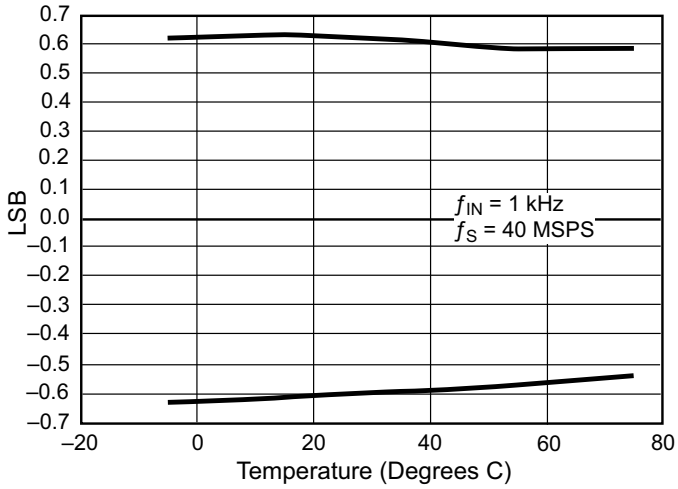
ILE Versus Sample Rate



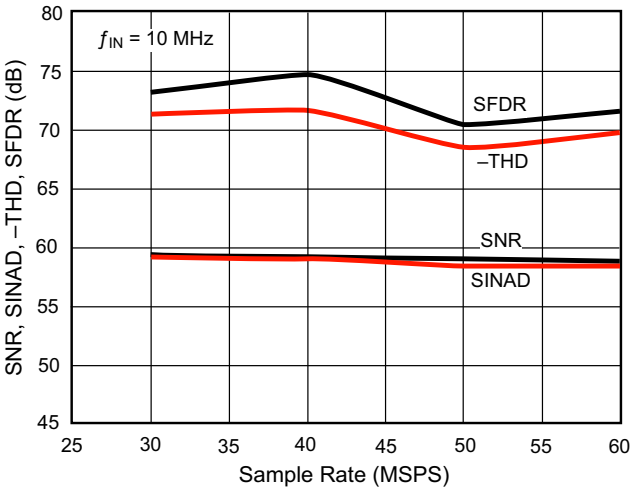
DLE Versus Temperature



ILE Versus Temperature



SNR, SINAD, –THD, SFDR Versus Sample Rate



SNR, SINAD, –THD, SFDR Versus Temperature

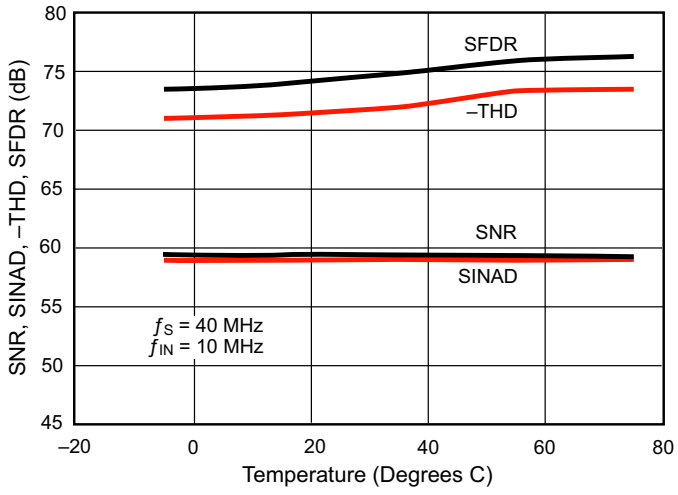
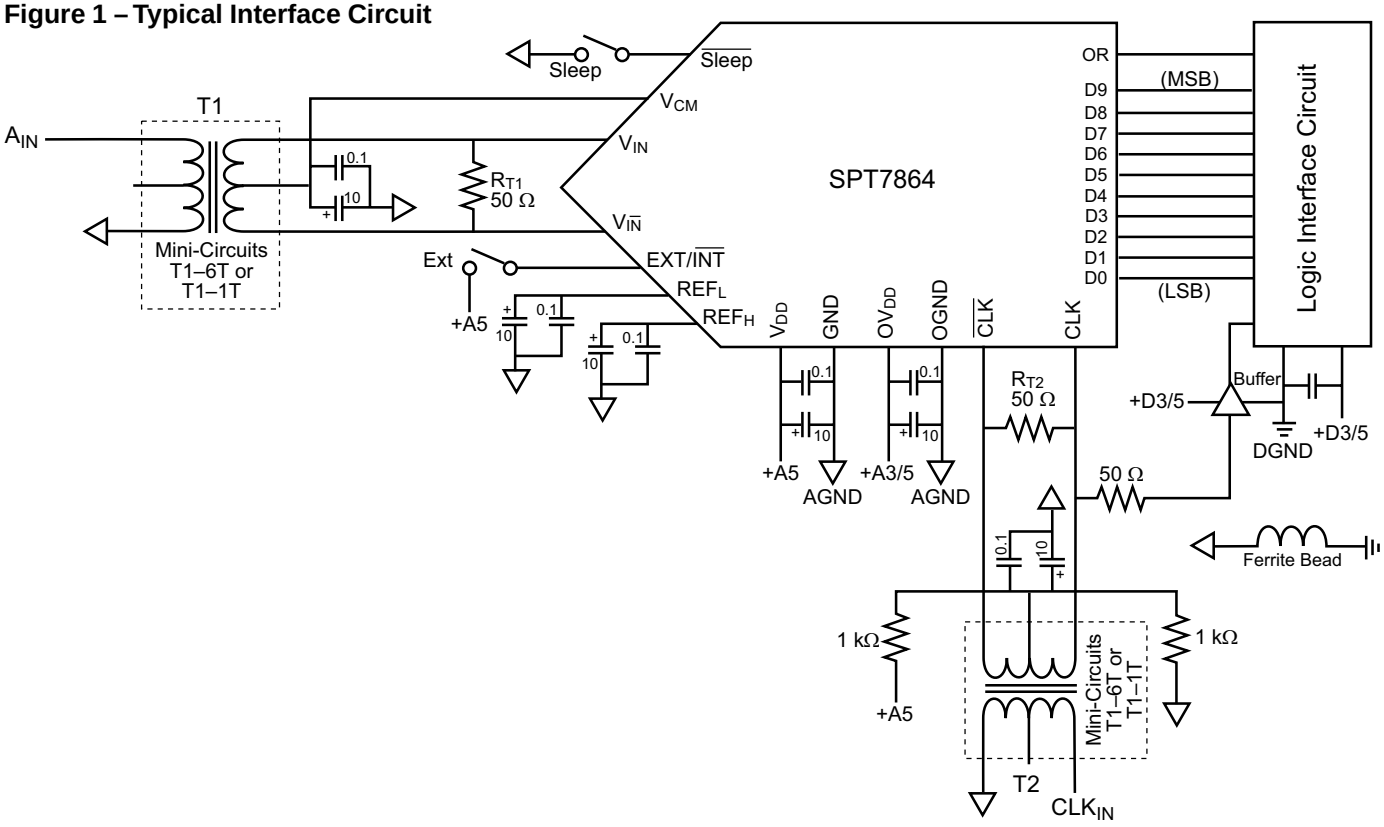


Figure 1 – Typical Interface Circuit



TYPICAL INTERFACE CIRCUIT

REFERENCES

The SPT7864 has a differential analog input. The input range is determined by the voltages V_{IN} and $V_{\overline{IN}}$ applied to reference pins REF_H and REF_L respectively, and is equal to $\pm(V_{IN}–V_{\overline{IN}})$. Externally generated reference voltages connected to REF_H and REF_L should be symmetric around 2.5 V. The input range can be defined between ±0.6 V and ±1.5 V. An internal reference exists, providing reference voltages at pins REF_H and REF_L equal to +3.0 V (V_{REFH}) and +2.0 V (V_{REFL}). These can be connected to REF_H and REF_L by connecting pin EXT/$\overline{INT}$ to GND. The references should be bypassed as close to the converter pins as possible using 100 nF capacitors in parallel with smaller capacitors (e.g. 220 pF) to ground.

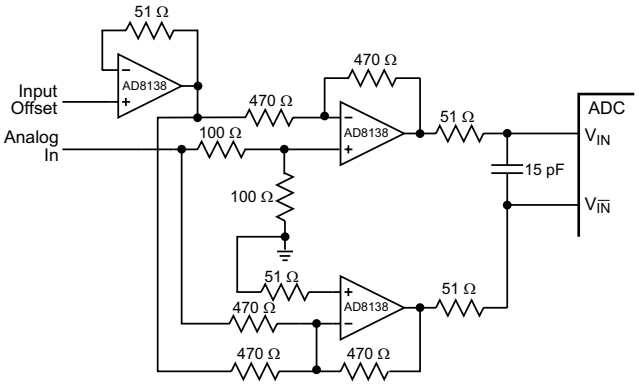
ANALOG INPUT

The input of the SPT7864 can be configured in various ways, dependent upon whether a single-ended or differential, AC- or DC-coupled input is wanted.

AC-coupled input is most conveniently implemented using a transformer with a center-tapped secondary winding. The center tap is connected to the V_{CM} node, as shown in figure 1. In order to obtain low distortion, it is important that the selected transformer does not exhibit core saturation at full scale. Excellent results are obtained with the Mini-Circuits T1-6T or T1-1T. Proper termination of the input is important for input signal purity. A small capacitor (typically 68 pF) across the inputs attenuates kickback noise from the sample-and-hold. A small capacitor (1 nF) between V_{CM} and ground has also been proven to be advantageous.

If a DC-coupled, single-ended input is wanted, a solution based on operational amplifiers, as shown in figure 2, is usually preferred. The AD8138 is suggested for low distortion and video bandwidth. Lower cost operational amplifiers may be used if the demands are less strict.

Figure 2 – DC-Coupled, Single-Ended to Differential Conversion (power supplies and bypassing not shown)



DIFFERENTIAL CLOCK INPUT

The SPT7864 clock can be driven differentially or single-ended. When driven differentially, $\overline{CLK}$ and CLK accommodate differential sinusodial signals centered around $V_{DD}/2$. The peak-to-peak value should be 0.8 V. In order to preserve accuracy at high input frequency, it is important that the clock have low jitter. The differential clock input is made to allow a low-jitter clock design. To ensure low jitter, the differential input should be a pure sine wave with low white noise floor.

SINGLE-ENDED CLOCK INPUT

For single-ended operation, the $\overline{CLK}$ node is internally biased to 1.5 V, and should externally be decoupled to ground by a capacitor. A CMOS logic level clock (5 V or 3 V) is applied at the CLK node. (To get an inverted clock input, CLK should be decoupled and the clock signal applied at the $\overline{CLK}$ node). The duty cycle of the clock should be close to 50%. Consecutive pipeline stages in the ADC are clocked in antiphase. With a 50% duty cycle, every stage has the same time for settling. If the duty cycle deviates from 50%, every second stage has a shorter time for settling; thus it operates less accurately, causing degradation of SNR.

In order to preserve accuracy at high input frequency, it is important that the clock have low jitter and steep edges. Rise/fall times should be kept shorter than 2 ns whenever possible. Overshoot should be minimized. Low jitter is especially important when converting high-frequency input signals. Jitter causes the noise floor to rise proportionally to input signal frequency. Jitter may be caused by crosstalk on the PCB. It is therefore recommended that the clock trace on the PCB be made as short as possible.

Figure 3 – Driving Differential Inputs with a Differential Configuration

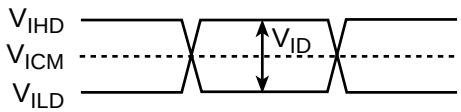
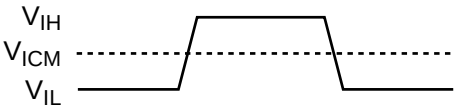


Figure 4 – Driving Differential Inputs with a Single-Ended Configuration



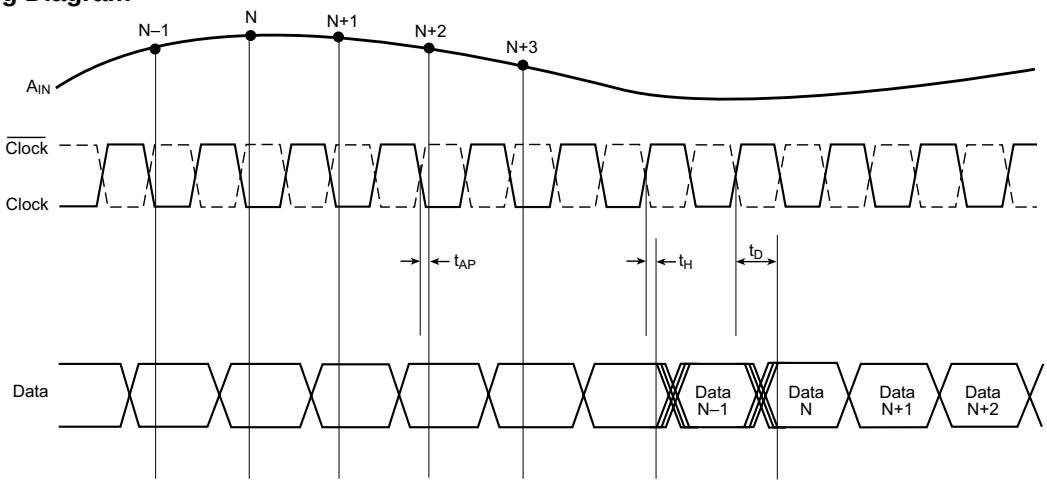
DIGITAL OUTPUTS

The digital output data appears in offset binary code at CMOS logic levels. Full-scale negative input results in output code 000...0. Full-scale positive input results in output code 111...1. Output data are available 6 clock cycles after the data are sampled. The analog input is sampled one aperture delay (t_{AP}) after the high-to-low clock transition. Output data should be sampled as shown in the timing diagram (figure 5). The OR pin is an out-of-range pin; if the outputs go either over or under range, OR is set high.

PCB LAYOUT AND DECOUPLING

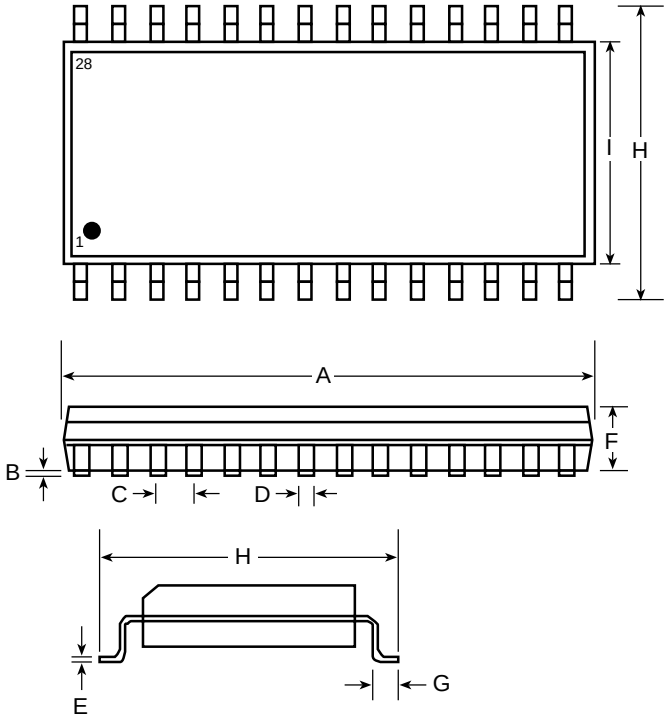
A well designed PCB is necessary to get good spectral purity from any high-performance ADC. A multilayer PCB with a solid ground plane is recommended for optimum performance. If the system has a split analog and digital ground plane, it is recommended that all ground pins on the ADC be connected to the analog ground plane. It is our experience that this gives the best performance. The power supply pins should be bypassed using 100 nF surface mounted capacitors as close to the package pins as possible. Analog and digital supply pins should be separately filtered.

Figure 5 – Timing Diagram



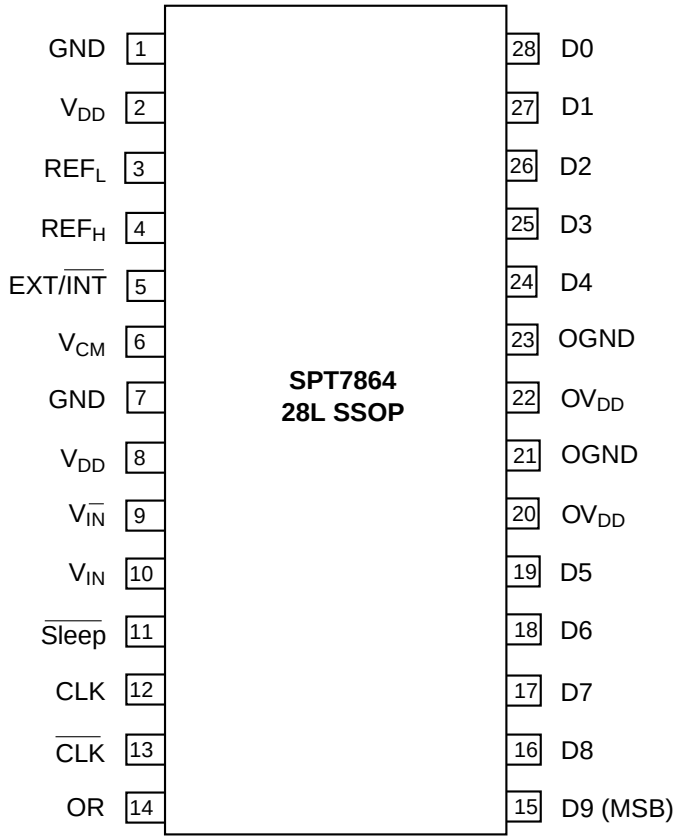
PACKAGE OUTLINE

28-Lead SSOP



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.390	0.413	9.90	10.50
B	0.002	0.008	0.05	0.20
C	0.026 typ		0.65 BSC	
D	0.009	0.015	0.22	0.38
E	0.004	0.010	0.09	0.25
F	0.065	0.073	1.65	1.85
G	0.022	0.037	0.55	0.95
H	0.291	0.323	7.40	8.20
I	0.197	0.220	5.00	5.60

PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
GND	Analog ground
V_{DD}	Analog +5 V
OGND	Output ground
OV_{DD}	Supply voltage for digital outputs 3 V/5 V
REF_L	Reference pin low, input for external reference, bypass with capacitor (10 µF) when internal reference is selected.
REF_H	Reference pin high, input for external reference, bypass with capacitor (10 µF) when internal voltage is selected.
V_{CM}	2.5 V common mode voltage reference output
V_{IN}	Non-inverted analog input
$V_{\overline{IN}}$	Inverted analog input
CLK	Clock input pin
$\overline{CLK}$	Complement of clock input pin, internally biased to 1.5 V; if single-ended clock is used, bypass to GND with 10 µF
D0–D9	Digital outputs; D0 = LSB; 3 V/5 V compatible
OR	Out-of-range bit; 3 V/5 V compatible
EXT/$\overline{INT}$	EXT/$\overline{INT}$ = 1, external reference used; internal reference powered down EXT/$\overline{INT}$ = 0, internal reference used; internally pulled down
$\overline{Sleep}$	$\overline{Sleep}$ = 1, normal operation; internally pulled up $\overline{Sleep}$ = 0, powered-down mode

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT7864SCR	0 to +70 °C	28L SSOP

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.