FAIRCHILD
SEMICONDUCTOR®

SPT7824

10-BIT, 40 MSPS, TTL OUTPUT A/D CONVERTER

FEATURES

- Monolithic 40 MSPS Converter
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- 57 dB SNR @ 3.58 MHz Input
- Low Power (1.0 W Typical)
- 5 pF Input Capacitance
- TTL Outputs

APPLICATIONS

- Medical Imaging
- Professional Video
- Radar Receivers
- Instrumentation
- Electronic Warfare
- Digital Communications

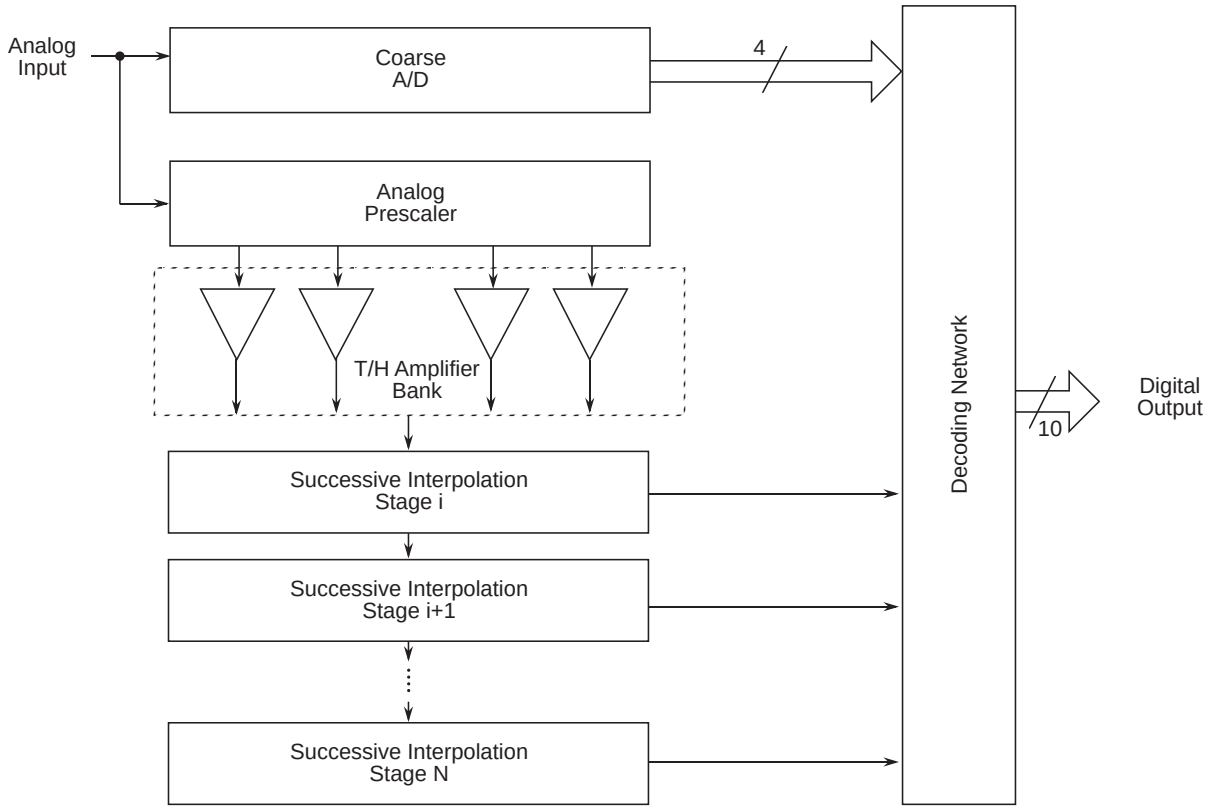
GENERAL DESCRIPTION

The SPT7824 A/D converter is a 10-bit monolithic converter capable of word rates a minimum of 40 MSPS. On board track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are TTL compatible to interface with TTL logic systems. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.0 watt with power supply voltages of +5.0 and -5.2 volts. The SPT7824 also provides a wide input voltage swing of ±2.0 volts.

The SPT7824 is available in 28-lead ceramic sidebrazed DIP, PDIP and SOIC packages over the commercial, industrial and military temperature ranges. Consult the factory for availability of die and /833 versions.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{CC} ..... +6 V
V_{EE} ..... -6 V

Input Voltages

Analog Input ..... $V_{FB} \leq V_{IN} \leq V_{FT}$
V_{FT}, V_{FB} ..... +3.0 V, -3.0 V
Reference Ladder Current ..... 12 mA
CLK Input ..... V_{CC}

Output

Digital Outputs ..... +30 to -30 mA

Temperature

Operating Temperature ..... -55 to +125 °C
Junction Temperature[1] ..... +175 °C
Lead Temperature, (soldering 10 seconds) ..... +300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ - T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{CLK}=40 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7824A MIN	SPT7824A TYP	SPT7824A MAX	SPT7824B MIN	SPT7824B TYP	SPT7824B MAX	UNITS
Resolution			10			10			Bits
DC Accuracy (+25 °C)	±Full Scale								
Integral Nonlinearity	100 kHz Sample Rate	V		±1.0			±1.5		LSB
Differential Nonlinearity		V		±0.5			±0.75		LSB
No Missing Codes		VI		Guaranteed			Guaranteed		
Analog Input	f_{CLK}=1 MHz								
Input Voltage Range		V		±2.0			±2.0		V
Input Bias Current	V_{IN}=0 V	VI		30	60	30		60	µA
Input Bias Current	T_A=-55 to +125 °C	IV			75			75	µA
Input Resistance		VI	100	300		100	300		kΩ
Input Resistance	T_A=-55 to +125 °C	IV	75	300		75	300		kΩ
Input Capacitance		V		5			5		pF
Input Bandwidth	3 dB Small Signal	V		120			120		MHz
+FS Error		V		±2.0			±2.0		LSB
-FS Error		V		±2.0			±2.0		LSB
Reference Input	f_{CLK}=1 MHz								
Reference Ladder Resistance		VI	500	800		500	800		Ω
Reference Ladder Tempco		V		0.8			0.8		Ω/°C
Timing Characteristics									
Maximum Conversion Rate		VI	40			40			MHz
Overvoltage Recovery Time		V		20			20		ns
Pipeline Delay (Latency)		IV			1			1	Clock Cycle
Output Delay	T_A=+25 °C	V		14	18	14		18	ns
Aperture Delay Time	T_A=+25 °C	V		1			1		ns
Aperture Jitter Time	T_A=+25 °C	V		5			5		ps-RMS
Acquisition Time	T_A=+25 °C	V		12			12		ns
Dynamic Performance									
Effective Number of Bits									
f_{IN}=1 MHz				8.7			8.2		Bits
f_{IN}=3.58 MHz				8.7			8.2		Bits
f_{IN}=10.0 MHz				7.3			6.9		Bits

Typical thermal impedances (unsoldered, in free air): 28L sidebrazed DIP: θ_{ja} = 50 °C/W, 28L plastic DIP: θ_{ja} = 50°C/W, 28L SOIC: θ_{ja} = 100 °C/W.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$-T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{CLK}=40 MHz, 50% clock duty cycle unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7824A MIN	SPT7824A TYP	SPT7824A MAX	SPT7824B MIN	SPT7824B TYP	SPT7824B MAX	UNITS
Dynamic Performance									
Signal-To-Noise Ratio (without Harmonics)									
f_{IN}=1 MHz	T_A=+25 °C	I	55	57		52	54		dB
	T_A=0 to +70, -25 to +85 °C	IV	53	55		50	52		dB
	T_A=-55 to +125 °C*	IV	49	51		46	48		dB
f_{IN}=3.58 MHz	T_A=+25 °C	I	55	57		52	54		dB
	T_A=0 to 70, -25 to +85 °C	IV	53	55		50	52		dB
	T_A=-55 to +125 °C*	IV	49	51		46	48		dB
f_{IN}=10.0 MHz	T_A=+25 °C	I	48	50		46	48		dB
	T_A=0 to 70, -25 to +85 °C	IV	45	47		43	45		dB
	T_A=-55 to +125 °C*	IV	41	43		39	41		dB
Harmonic Distortion									
f_{IN}=1 MHz	T_A=+25 °C	I	54	56		52	54		dB
	T_A=0 to 70, -25 to +85 °C	IV	51	53		49	51		dB
	T_A=-55 to +125 °C*	IV	50	52		48	50		dB
f_{IN}=3.58 MHz	T_A=+25 °C	I	54	56		52	54		dB
	T_A=0 to 70, -25 to +85 °C	IV	51	53		49	51		dB
	T_A=-55 to +125 °C*	IV	50	52		48	50		dB
f_{IN}=10.0 MHz	T_A=+25 °C	I	46	48		43	45		dB
	T_A=0 to 70, -25 to +85 °C	IV	45	47		41	44		dB
	T_A=-55 to +125 °C*	IV	44	46		40	42		dB
Signal-to-Noise and Distortion									
f_{IN}=1 MHz	T_A=+25 °C	I	52	54		49	51		dB
	T_A=0 to 70, -25 to +85 °C	IV	49			46			dB
	T_A=-55 to +125 °C*	IV	48			45			dB
f_{IN}=3.58 MHz	T_A=+25 °C	I	52	54		49	51		dB
	T_A=0 to 70, -25 to +85 °C	IV	49			46			dB
	T_A=-55 to +125 °C*	IV	48			45			dB
f_{IN}=10.0 MHz	T_A=+25 °C	I	44	46		41	43		dB
	T_A=0 to 70, -25 to +85 °C	IV	43			40			dB
	T_A=-55 to +125 °C*	IV	40			37			dB
Spurious Free Dynamic Range	T_A=+25 °C, f_{IN}=1 MHz	V		67			67		dB
Differential Phase	T_A=+25 °C, f_{IN} = 3.58 & 4.35 MHz	V		0.2			0.2		Degree
Differential Gain	T_A=+25 °C, f_{IN} = 3.58 & 4.35 MHz	V		0.5			0.7		%
Digital Inputs	f_{CLK}=1 MHz								
Logic 1 Voltage		VI	2.4		4.5	2.4		4.5	V
Logic 0 Voltage		VI			0.8			0.8	V
Maximum Input Current Low	T_A=+25 °C	I	0	+5	+20	0	+5	+20	µA
Maximum Input Current High	T_A=+25 °C	I	0	+5	+20	0	+5	+20	µA
Pulse Width Low (CLK)		IV	10			10			ns
Pulse Width High (CLK)		IV	10		300	10		300	ns
Digital Outputs	f_{CLK}=1 MHz								
Logic "1" Voltage		VI	2.4			2.4			V
Logic "0" Voltage		VI			0.6			0.6	V
Power Supply Requirements									
Voltages V_{CC}		IV	4.75		5.25	4.75		5.25	V
DV_{CC}		IV	4.75	5.0	5.25	4.75	5.0	5.25	V
$-V_{EE}$		IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	V
Currents I_{CC}	T_A=+25 °C	I		118	145		118	145	mA
DI_{CC}	T_A=+25 °C	I		40	55		40	55	mA
$-I_{EE}$	T_A=+25 °C	I		40	57		40	57	mA
Power Dissipation	T_A=+25 °C	I		1.0	1.3		1.0	1.3	W
Power Supply Rejection	+5 V ±0.25 V, -5.2 V ±0.25 V	V		1.0			1.0		LSB

*****Temperature tested /883 only.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A - Timing Diagram

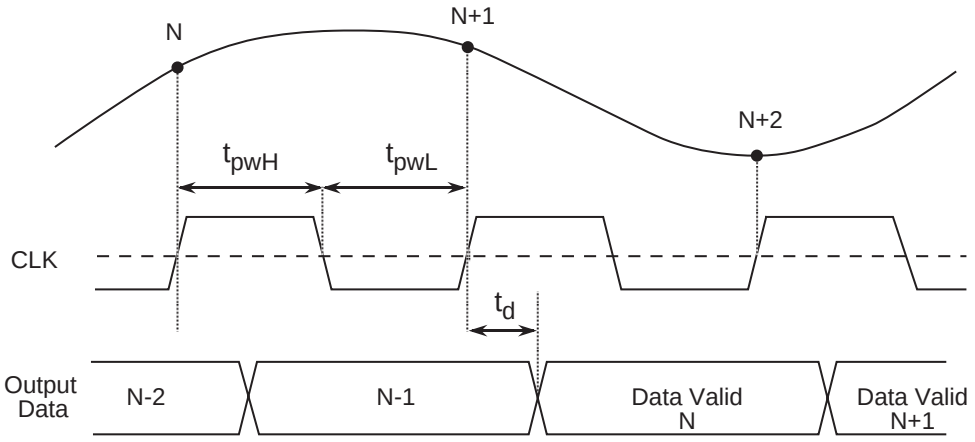


Figure 1B - Single Event Clock

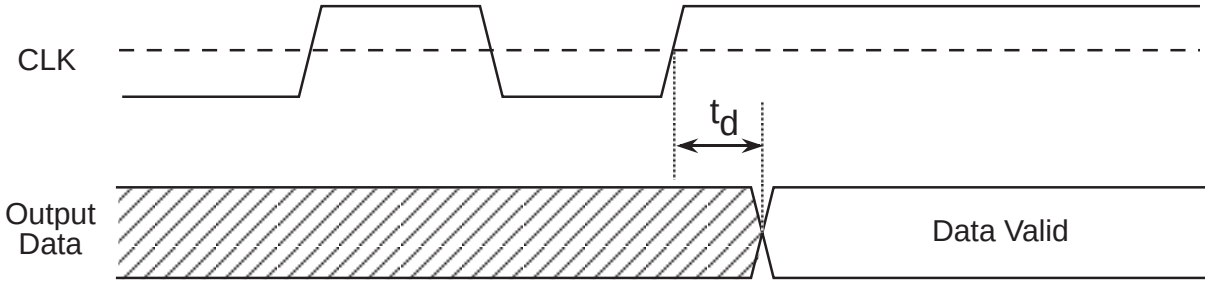
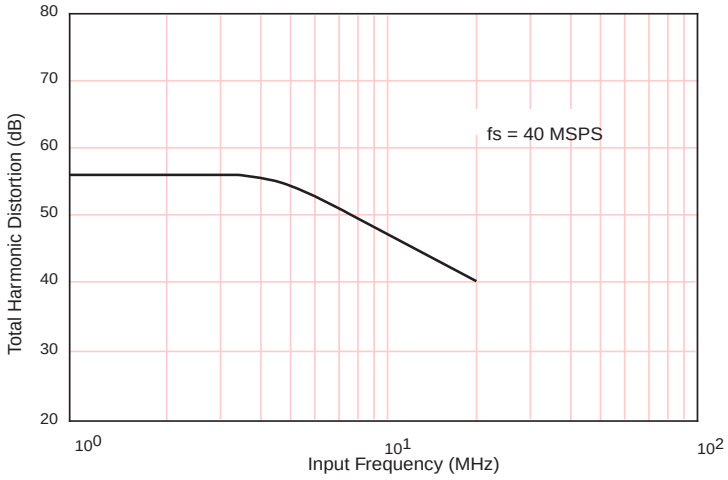


Table I - Timing Parameters

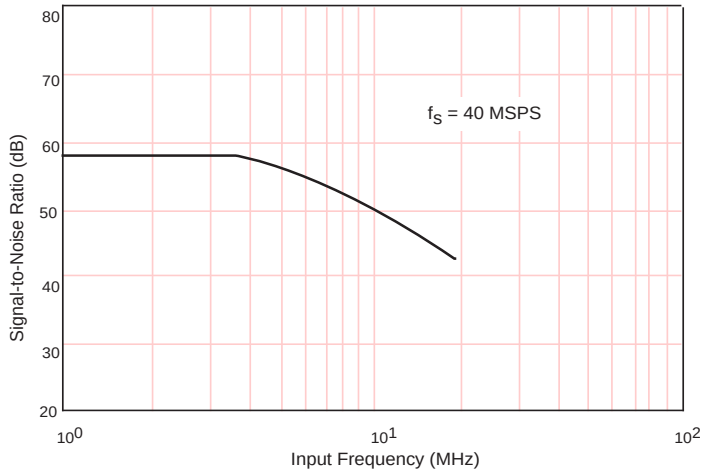
PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Prop Delay	-	14	18	ns
t_{pwH}	CLK High Pulse Width	10	-	300	ns
t_{pwL}	CLK Low Pulse Width	10	-	-	ns

TYPICAL PERFORMANCE CHARACTERISTICS

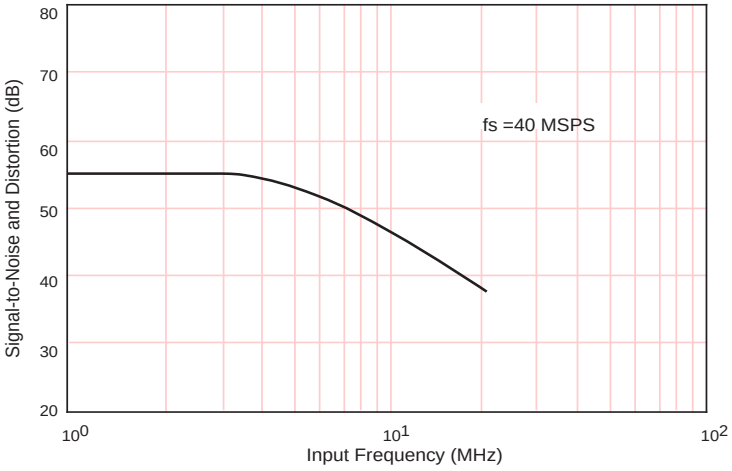
THD vs Input Frequency



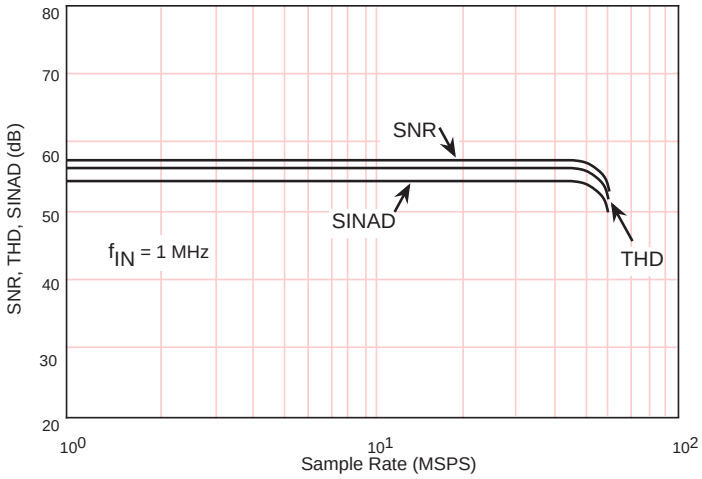
SNR vs Input Frequency



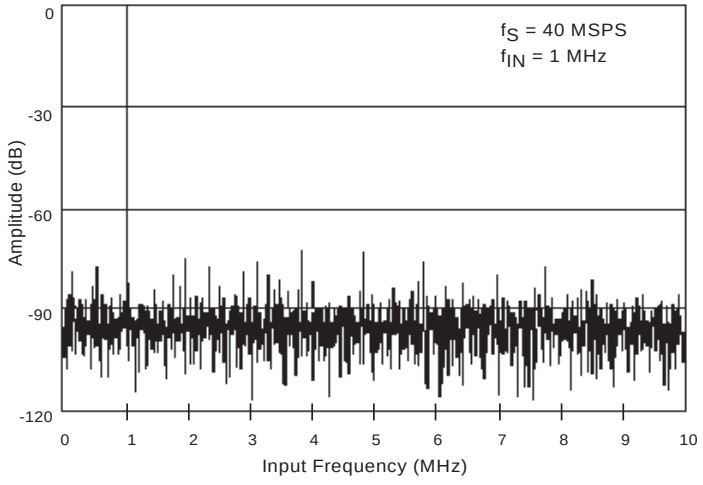
SINAD vs Input Frequency



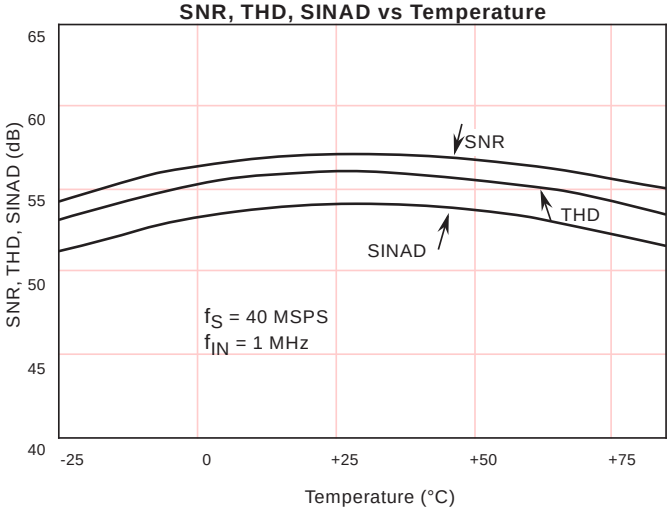
SNR, THD, SINAD vs Sample Rate



Spectral Response



SNR, THD, SINAD vs Temperature



TYPICAL INTERFACE CIRCUIT

The SPT7824 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7824 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

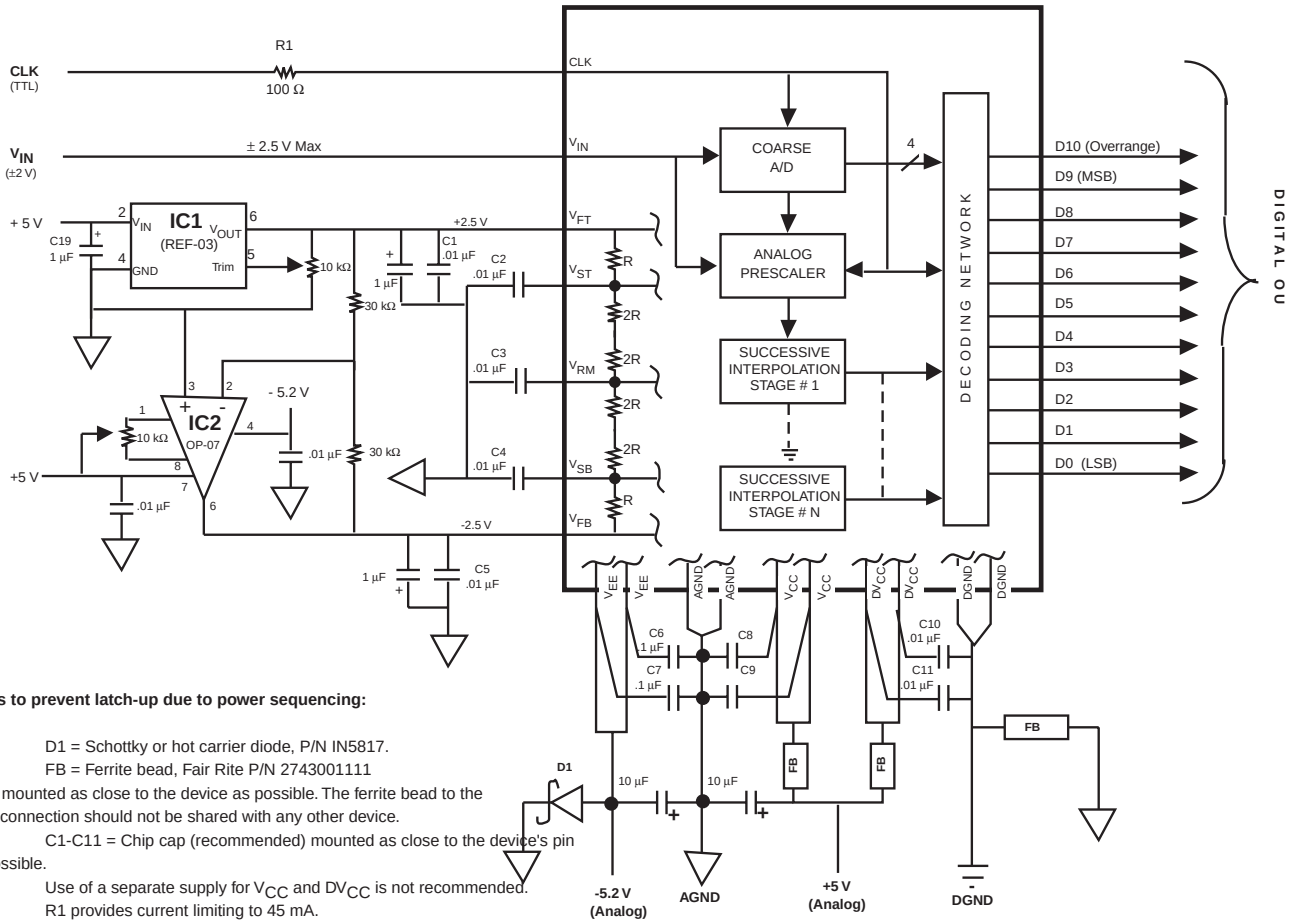
POWER SUPPLIES AND GROUNDING

The SPT7824 requires -5.2 V and +5 V analog supply voltages. The +5 V supply is common to analog V_{CC} and digital DV_{CC}. A ferrite bead in series with each supply line is intended to reduce the transient noise injected into the analog V_{CC}. These beads should be connected as closely as possible to the device. The connection between the beads and the SPT7824 should not be shared with any other device. Each power supply pin should be bypassed as closely as possible to the device. Use 0.1 µF for V_{EE} and V_{CC}, and 0.01 µF for DV_{CC} (chip caps are preferred).

AGND and DGND are the two grounds available on the SPT7824. These two internal grounds are isolated on the device. The use of ground planes is recommended to achieve optimum device performance. DGND is needed for the DV_{CC} return path (40 mA typical) and for the return path for all digital output logic interfaces. AGND and DGND should be separated from each other and connected together only at the device through a ferrite bead.

A Schottky or hot carrier diode connected between AGND and V_{EE} is required. The use of separate power supplies between V_{CC} and DV_{CC} is not recommended due to potential power supply sequencing latch-up conditions. Using the recommended interface circuit shown in figure 2 will provide optimum device performance for the SPT7824.

Figure 2 - Typical Interface Circuit



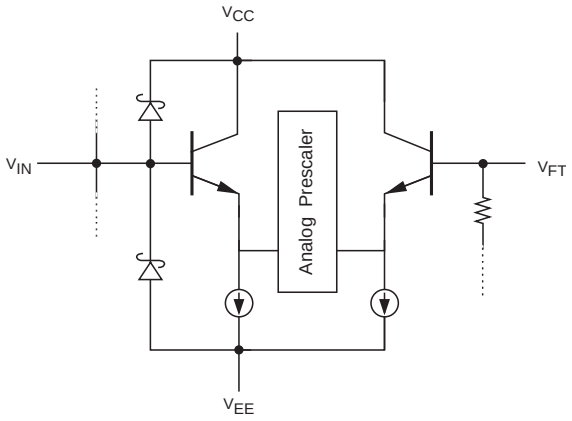
Notes to prevent latch-up due to power sequencing:

1) D1 = Schottky or hot carrier diode, P/N IN5817.
2) FB = Ferrite bead, Fair Rite P/N 2743001111
to be mounted as close to the device as possible. The ferrite bead to the ADC connection should not be shared with any other device.
3) C1-C11 = Chip cap (recommended) mounted as close to the device's pin as possible.
4) Use of a separate supply for V_{CC} and DV_{CC} is not recommended.
5) R1 provides current limiting to 45 mA.
6) C6, C7, C8 and C9 should be ten times larger than C10 and C11.
7) C8 = C9 = a 0.1 µF cap in parallel with a 4.7 µF cap.

VOLTAGE REFERENCE

The SPT7824 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 ohms. The +2.5 V voltage source for reference V_{FT} must be current limited to 20 mA maximum if a different driving circuit is used in place of the recommended reference circuit shown in figures 2 and 3. In addition, there are three reference ladder taps (V_{ST}, V_{RM} and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RM} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). These points should be used to monitor the actual full scale input voltage of the device and should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF (chip carrier preferred) connected to AGND from each tap is recommended to minimize high frequency noise injection.

Figure 3 - Analog Equivalent Input Circuit



An example of a reference driver circuit recommended is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a tolerance of 0.6% or +/- 0.015 V. The potentiometer R1 is 10 kΩ and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. V_{FT} and V_{FB} should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0 V respectively.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with ± 2.5 V references, the accuracy of the device will degrade if operated beyond a ± 2% range.

The following errors are defined:
+FS error = top of ladder offset voltage = Δ(+FS -V_{ST}+1 LSB)
-FS error = bottom of ladder offset voltage = Δ(-FS-V_{SB}-1LSB)
where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

ANALOG INPUT

V_{IN} is the analog input. The full scale input range will be 80% of the reference voltage or ±2 V with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

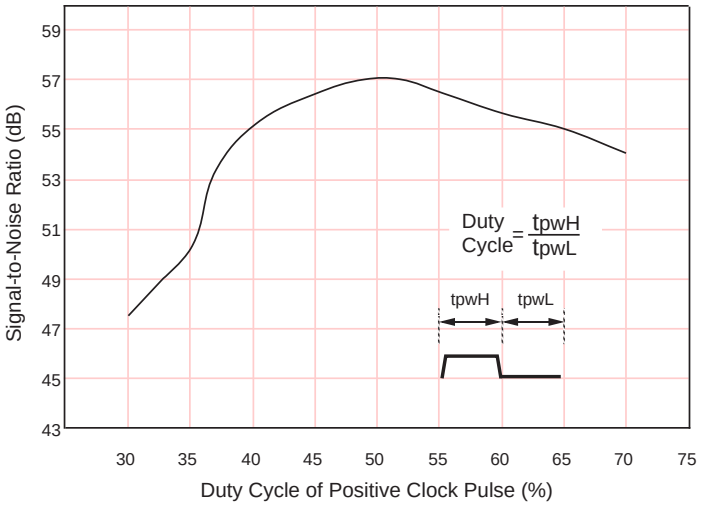
The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due to the SPT7824's extremely low input capacitance of only 5 pF and very high input resistance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 μA.

CLOCK INPUT

The SPT7824 is driven from a single-ended TTL input (CLK). The CLK pulse width (tpwH) must be kept between 10 ns and 300 ns to ensure proper operation of the internal track-and-hold amplifier. (See timing diagram.) When operating the SPT7824 at sampling rates above 3 MSPS, it is recommended that the clock input duty cycle be kept at 50% to optimize performance. (See figure 4.) The analog input signal is latched on the rising edge of the CLK.

The clock input must be driven from fast TTL logic (V_{IH} ≤4.5 V, T_{RISE} <6 ns). In the event the clock is driven from a high current source, use a 100 Ω resistor in series to current limit to approximately 45 mA.

Figure 4 - SNR vs Clock Duty Cycle



DIGITAL OUTPUTS

The format of the output data (D0-D9) is straight binary. (See table II.) The outputs are latched on the rising edge of CLK with a propagation delay of 14 ns (typ). There is a one clock cycle latency between CLK and the valid output data. (See timing diagram.)

Table II - Output Data Information

ANALOG INPUT	OVERRANGE D1O	OUTPUT CODE D9-DO
>+2.0 V + 1/2 LSB	1	11 1111 1111
+2.0 V -1 LSB	O	11 1111 111Ø
0.0 V	O	ØØ ØØØØ ØØØØ
-2.0 V +1 LSB	O	OO OOOO OOOØ
<-2.0 V	O	OO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

The rise times and fall times of the digital outputs are not symmetrical. The propagation delay of the rise time is typically 14 ns and the fall time is typically 6 ns. (See figure 5.) The nonsymmetrical rise and fall times create approximately 8 ns of invalid data.

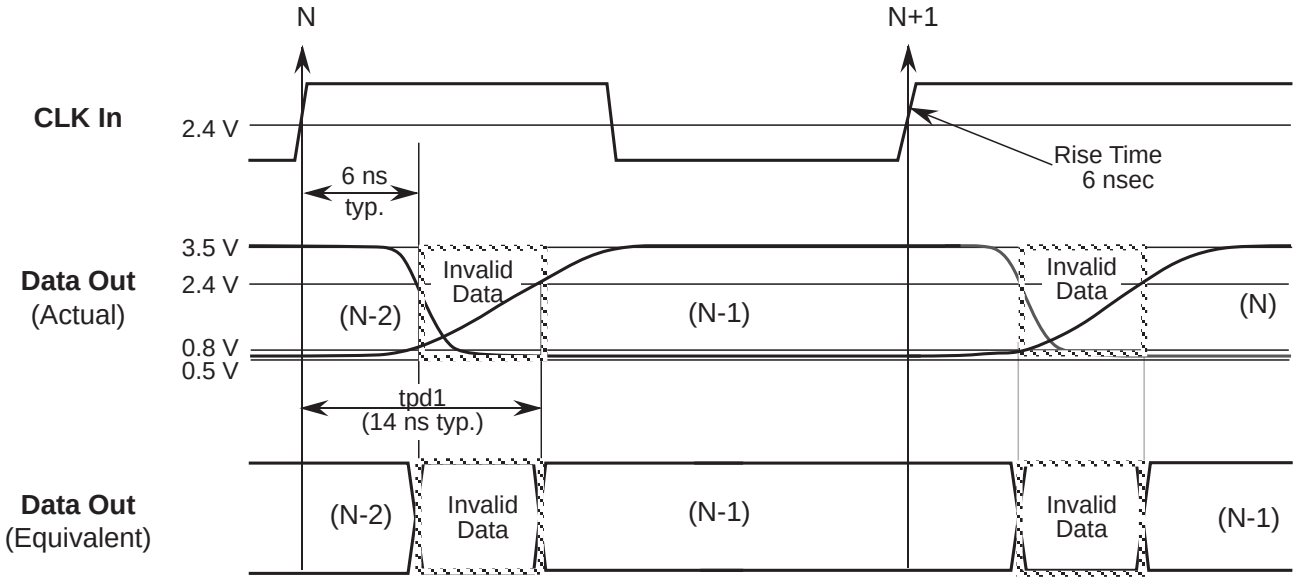
OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7824 into higher resolution systems.

EVALUATION BOARD

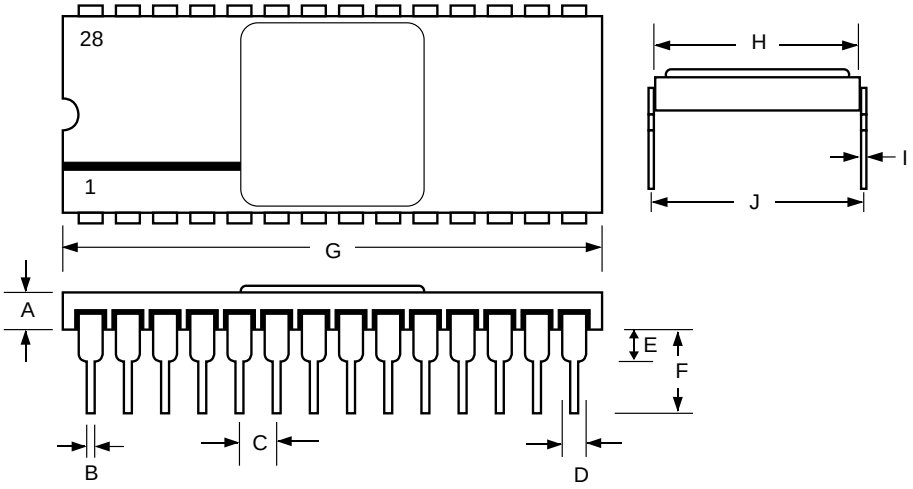
The EB7824 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7824. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7824 is also available. Contact the factory for price and availability.

Figure 5 - Digital Output Characteristics



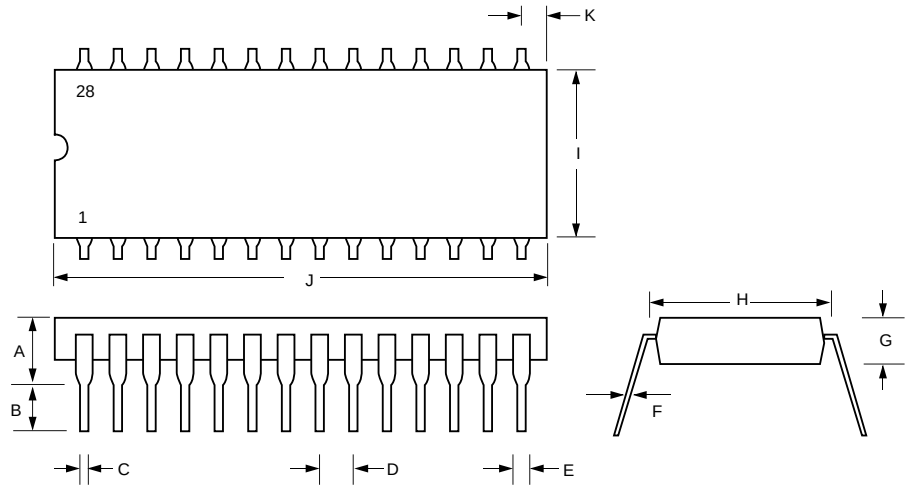
PACKAGE OUTLINES

28-Lead Sidebrazed



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.077	0.093	1.96	2.36
B	0.016	0.020	0.41	0.51
C	0.095	0.105	2.41	2.67
D		.050 typ	0.00	1.27
E	0.040	0.060	1.02	1.52
F	0.215	0.235	5.46	5.97
G	1.388	1.412	35.26	35.86
H	0.585	0.605	14.86	15.37
I	0.009	0.012	0.23	0.30
J	0.600	0.620	15.24	15.75

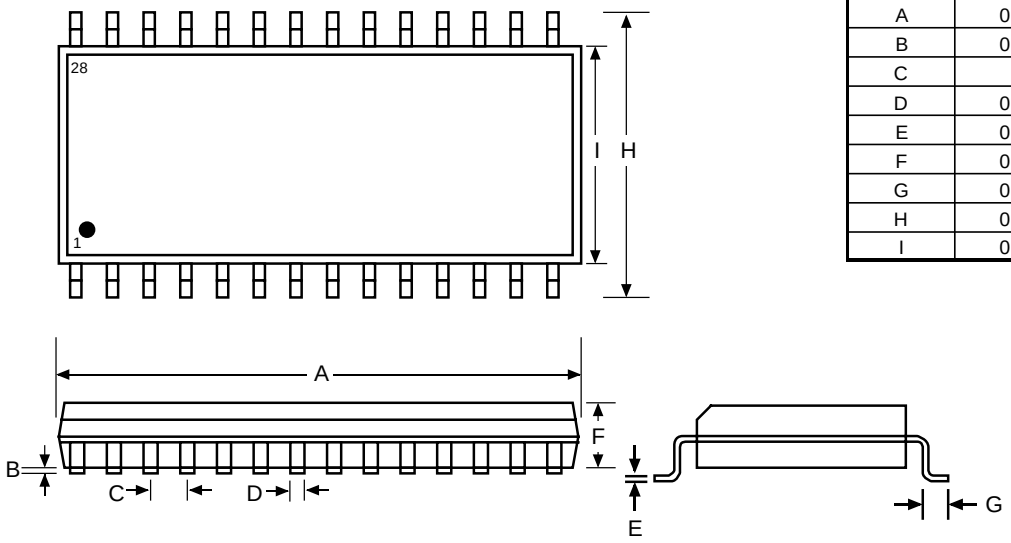
28-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.200		5.08
B	0.120	0.135	3.05	3.43
C		0.020		0.51
D		0.100		2.54
E		0.067		1.70
F		0.013		0.33
G	0.170	0.180	4.32	4.57
H		0.622		15.80
I		0.555		14.10
J		1.460		37.08
K		0.085		2.16

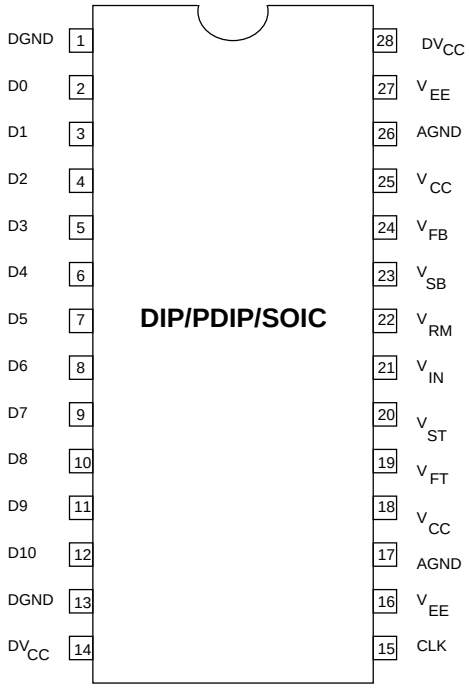
PACKAGE OUTLINES

28-Lead SOIC



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.696	0.712	17.68	18.08
B	0.004	0.012	0.10	0.30
C		.050 typ	0.00	1.27
D	0.014	0.019	0.36	0.48
E	0.009	0.012	0.23	0.30
F	0.080	0.100	2.03	2.54
G	0.016	0.050	0.41	1.27
H	0.394	0.419	10.01	10.64
I	0.291	0.299	7.39	7.59

PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
DGND	Digital Ground
D0-D9	TTL Outputs (D0=LSB)
D10	TTL Output Overrange
CLK	Clock
V_{EE}	-5.2 V Supply (Analog)
AGND	Analog Ground
V_{CC}	+5.0 V Supply (Analog)
V_{IN}	Analog Input
DV_{CC}	Digital +5.0 V Supply
V_{RM}	Middle of Voltage Reference Ladder
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT7824AIJ	-25 to +85 °C	28L Sidebrazed DIP
SPT7824BIJ	-25 to +85 °C	28L Sidebrazed DIP
SPT7824ACN	0 to +70 °C	28L Plastic DIP
SPT7824BCN	0 to +70 °C	28L Plastic DIP
SPT7824ACS	0 to +70 °C	28L SOIC
SPT7824BCS	0 to +70 °C	28L SOIC
SPT7824AMJ	-55 to +125 °C	28L Sidebrazed DIP
SPT7824BMJ	-55 to +125 °C	28L Sidebrazed DIP