FAIRCHILD
SEMICONDUCTOR®

SPT7750

8-BIT, 500 MSPS, FLASH A/D CONVERTER

OCTOBER 2002

FEATURES

- 1:2 Demuxed ECL compatible outputs
- Wide input bandwidth – 900 MHz
- Low input capacitance – 15 pF
- Metastable errors reduced to 1 LSB
- Monolithic for low cost
- Gray code output

APPLICATIONS

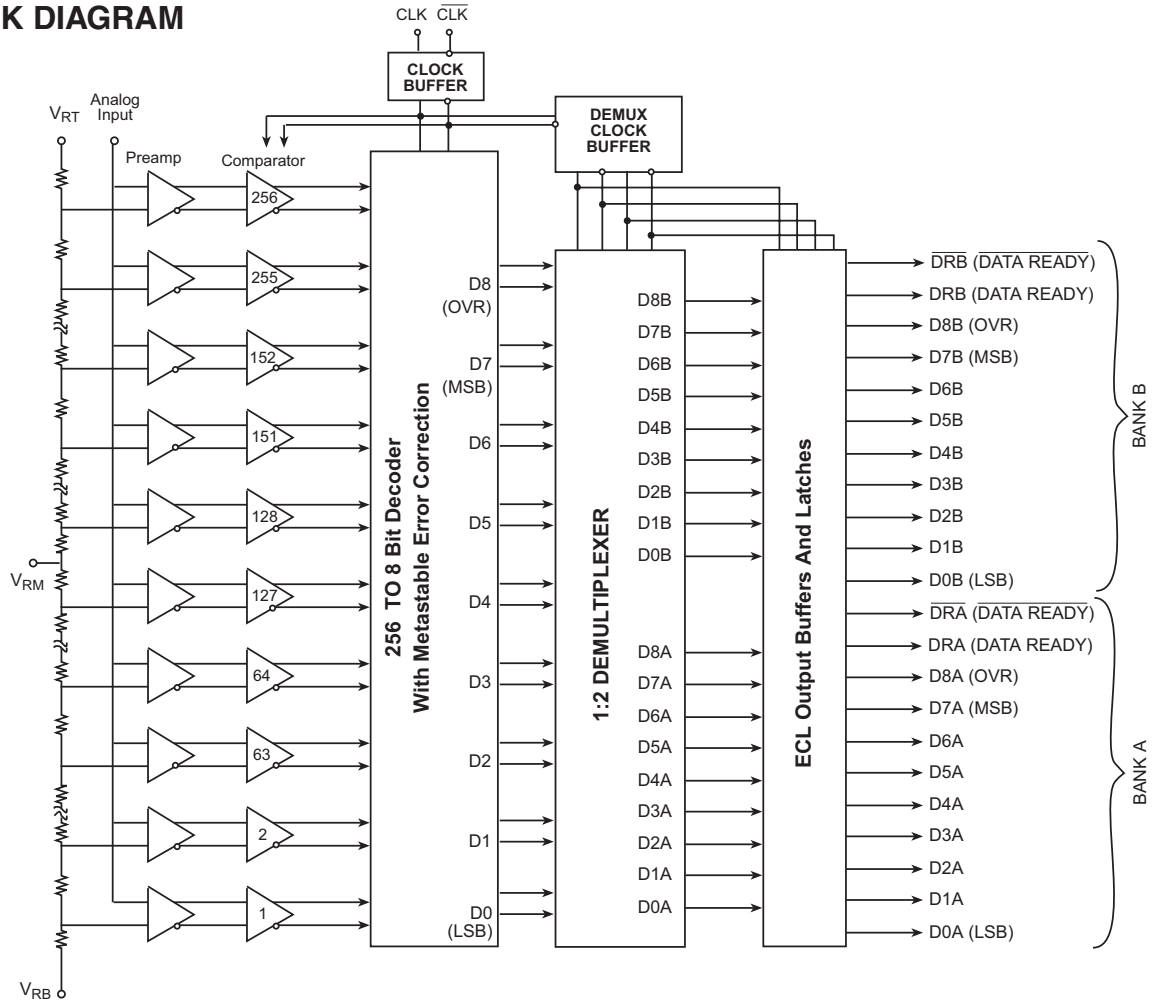
- Digital oscilloscopes
- Transient capture
- Radar, EW, ECM
- Direct RF down-conversion

GENERAL DESCRIPTION

The SPT7750 is a full parallel (flash) analog-to-digital converter capable of digitizing full scale (0 to –2 V) inputs into eight-bit digital words at an update rate of 500 MSPS. The ECL-compatible outputs are demultiplexed into two separate output banks, each with differential data ready outputs to ease the task of data capture. The SPT7750's wide input bandwidth and low capacitance eliminate the need for external track-and-hold amplifiers for most applications. A proprietary decoding scheme reduces metastable errors to the 1 LSB level. The SPT7750 operates from a single –5.2 V supply, with a nominal power dissipation of 5.5 W.

The SPT7750 is available in an 80-lead surface-mount MQuad package over the industrial temperature range (–25 °C to +85 °C).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

Negative Supply Voltage (V_{EE} TO GND) –7.0 to +0.5 V
Ground Voltage Differential ..... –0.5 to +0.5 V

Input Voltage

Analog Input Voltage ..... +0.5 V to V_{EE}
Reference Input Voltage ..... +0.5 V to V_{EE}
Digital Input Voltage ..... +0.5 V to V_{EE}
Reference Current V_{RT} to V_{RB} ..... 35 mA

Output

Digital Output Current ..... 0 to –28 mA

Temperature

Operating Temperature, ambient .....–25 to +85 °C
case .....+125 °C
junction .....+150 °C
Lead Temperature, (soldering 10 seconds) .....+300 °C
Storage Temperature .....–65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_J = T_C = T_A = +25$ °C , V_{EE}=–5.2 V, V_{RB}=–2.0 V, V_{RM}=–1.0 V, V_{RT}=0.00 V, f_{CLK}=500 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7750A MIN	SPT7750A TYP	SPT7750A MAX	SPT7750B MIN	SPT7750B TYP	SPT7750B MAX	UNITS
Resolution				8			8		Bits
DC Accuracy									
Integral Linearity Error (ILE)	f_{CLK} = 100 kHz	I	–1.0		+1.0	–1.5		+1.5	LSB
Differential Linearity Error (DLE)	f_{CLK} = 100 kHz	I	–0.85		+0.95	–0.95		+1.5	LSB
No Missing Codes			Guaranteed			Guaranteed			
Analog Input									
Input Voltage Range		I	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
Input Bias Current	V_{IN}=0 V	I		.75	2.0		.75	2.0	mA
Input Resistance		V		15			15		kΩ
Input Capacitance	Over Full Input Range	V		15			15		pF
Input Bandwidth									
Small Signal		V		900			900		MHz
Large Signal		V		500			500		MHz
Offset Error V_{RT}		IV	–30		+30	–30		+30	mV
Offset Error V_{RB}		IV	–30		+30	–30		+30	mV
Input Slew Rate		V		5			5		V/ns
Clock Synchronous Input Currents		V		2			2		µA
Reference Input									
Ladder Resistance		I	60	80		60	80		Ω
Reference Bandwidth		V		30			30		MHz
Timing Characteristics									
Maximum Sample Rate		I	500			500			MHz
Aperture Jitter		V		2			2		ps
Acquisition Time		V		250			250		ps
Clock to Data Delay		IV	0.9	1.4	1.9	0.9	1.4	1.9	ns
CLK to Data Ready Delay		IV	1.25	1.75	2.25	1.25	1.75	2.25	ns
Dynamic Performance									
Signal-To-Noise Ratio (without Harmonics)									
f_{IN} = 50 MHz		I	47			45			dB
f_{IN} = 250 MHz		I	44			42			dB
Total Harmonic Distortion									
f_{IN} = 50 MHz		I	–46			–44			dBc
f_{IN} = 250 MHz		I	–38			–36			dBc
Signal-to-Noise and Distortion									
f_{IN} = 50 MHz		I	43			41			dB
f_{IN} = 250 MHz		I	37			35			dB

ELECTRICAL SPECIFICATIONS

$T_J = T_C = T_A = +25$ °C , V_{EE}=–5.2 V, V_{RB}=–2.0 V, V_{RM}=–1.0 V, V_{RT}=0.00 V, f_{CLK}=500 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7750A MIN	SPT7750A TYP	SPT7750A MAX	SPT7750B MIN	SPT7750B TYP	SPT7750B MAX	UNITS
Dynamic Performance									
Spurious Free Dynamic Range									
f_{IN} = 50 MHz		I	49			44			dB
f_{IN} = 250 MHz		I	41			36			dB
Digital Inputs									
Input High Voltage									
(CLK, $\overline{CLK}$)		I	–1.1	–0.7		–1.1	–0.7		V
Input Low Voltage									
(CLK, $\overline{CLK}$)		I		–1.8	–1.5		–1.8	–1.5	V
Clock Pulse Width High (t_{PWH})		I	1.0	0.67		1.0	0.67		ns
Clock Pulse Width Low (t_{PWL})		I	1.0	0.67		1.0	0.67		ns
Digital Outputs									
Logic 1 Voltage		I	–1.1	–0.9		–1.1	–0.9		V
Logic 0 Voltage		I		–1.8	–1.5		–1.8	–1.5	V
Rise Time	20% to 80%	V		450			450		ps
Fall Time	20% to 80%	V		450			450		ps
Power Supply Requirements									
Voltage V_{EE}		IV	–4.95	–5.2	–5.45	–4.95	–5.2	–5.45	V
Current I_{EE}		I		1.05	1.2		1.05	1.2	A
Power Dissipation		I		5.5	6.25		5.5	6.25	W

Typical Thermal Impedance: θ_{JC} = +4 °C/W.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all test are pulsed tests; therefore, $T_J = T_C = T_A$.

LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

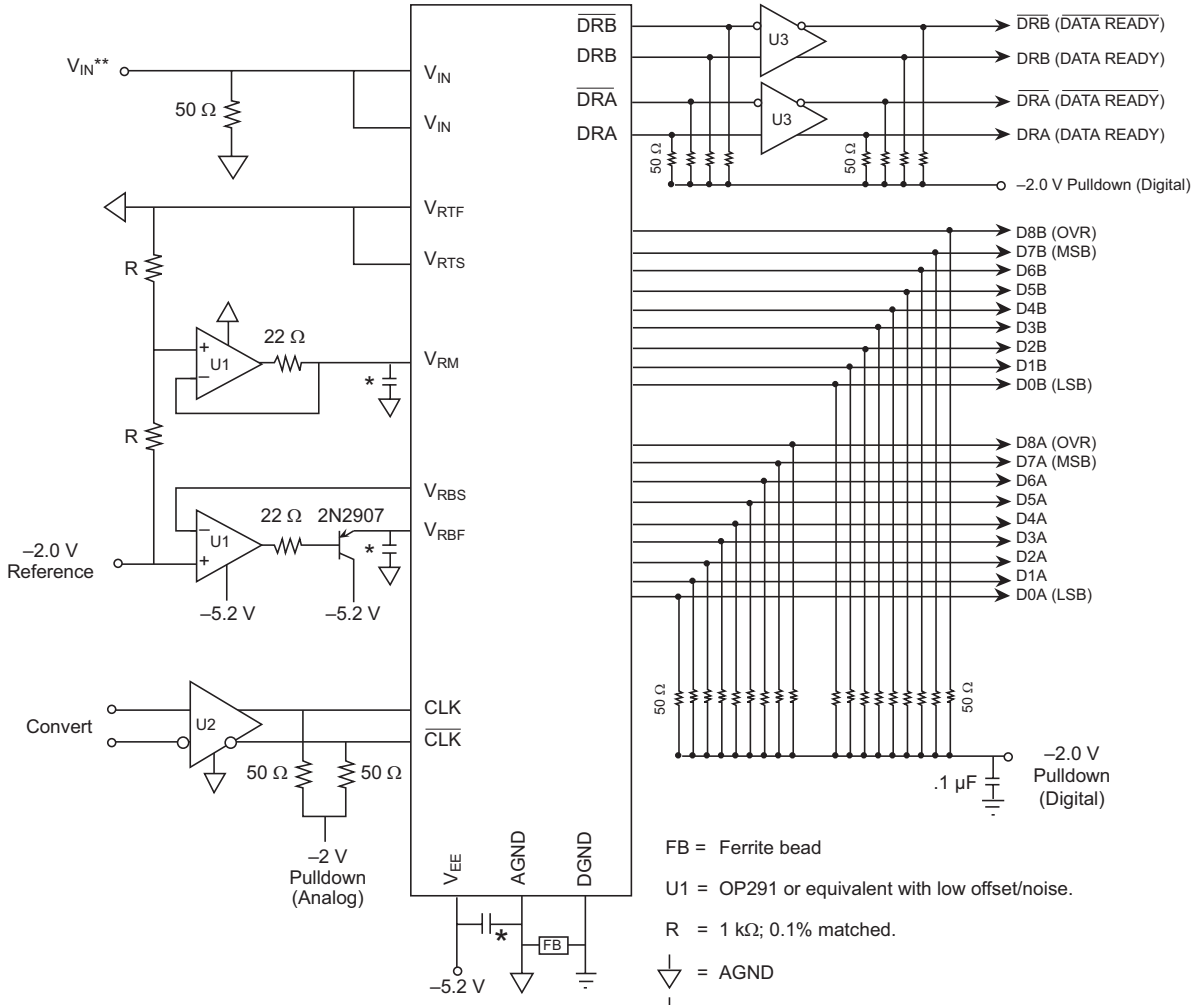
GENERAL DESCRIPTION

The SPT7750 is one of the fastest monolithic 8-bit parallel flash A/D converters available today. The nominal conversion rate is 500 MSPS and the analog bandwidth is in excess of 900 MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators (see block diagram). This not only reduces clock transient kickback to the input and reference ladder due to a low AC beta, but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so that it remains constant over different input voltage and frequency ranges and therefore makes the part easier to drive than previous flash converters. The preamplifiers also add a gain of two to the input signal so that each comparator has a wider overdrive or threshold range to "trip" into or out of the active state. This gain reduces metastable states that can cause errors at the output.

The SPT7750 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. The output drive capability of the device can provide full ECL swings into 50 Ω loads.

Figure 1 – SPT7750 Typical Interface Circuit



FB = Ferrite bead

U1 = OP291 or equivalent with low offset/noise.

R = 1 kΩ; 0.1% matched.

= AGND

= DGND

U2 = ON Semiconductor ECLinPS LITE, MC10EL16, differential receiver with 250 ps (typ) propagation delay.

U3 = MC10EL16 or MC100EL16.

* = 10 µF Tantalum Capacitor and 0.1 µF Chip Capacitor

** = Care must be taken to avoid exceeding the maximum rating for the input, especially during power up sequencing of the analog input driver.

TYPICAL INTERFACE CIRCUIT

The circuit in figure 1 is intended to show the most elaborate method of achieving the least error by correcting for integral linearity, input induced distortion, and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, input buffer, and supply decoupling. Please contact the factory for the SPT7750 evaluation board application note that contains more details on interfacing the SPT7750. The function of each pin and external connections to other components is as follows:

V_{EE}, AGND, DGND

V_{EE} is the supply pin with AGND as ground for the device. The power supply pins should be bypassed as close to the device as possible with at least a .01 μF ceramic capacitor. A 10 μF tantalum can also be used for low frequency suppression. DGND is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in figure 1.

V_{IN} (ANALOG INPUT)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input sense and the other for input force. This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The SPT7750 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion.

CLK, $\overline{CLK}$ (CLOCK INPUTS)

The clock inputs are designed to be driven differentially with ECL levels. The duty cycle of the clock should be kept at 50% to avoid causing larger second harmonics. If this is not important to the intended application, then duty cycles other than 50% may be used.

D0 TO D8, DR, $\overline{DR}$, (A AND B)

The digital outputs can drive 50 Ω to ECL levels when pulled down to –2 V. When pulled down to –5.2 V, the outputs can drive 130 Ω to 1 kΩ loads. All digital outputs are grey code with the coding as shown in table I. Fairchild recommends using differential receivers on the outputs of the data ready lines to ensure the proper output rise and fall times.

V_{RBF}, V_{RBS}, V_{RTF}, V_{RTS}, V_{RM} (REFERENCE INPUTS)

There are two reference inputs and one external reference voltage tap. These are –2 V (V_{RB} force and sense), midtap (V_{RM}) and AGND (V_{RT} force and sense). The reference pins and tap can be driven by op amps as shown in figure 1 or V_{RM} may be bypassed for limited temperature operation. These voltage inputs can be bypassed to AGND for further noise suppression if so desired.

Table I – Output Coding

V_{IN}	D8	D7 . . . D8
>–0.5 LSB	1	1 0 0 0 0 0 0 0
–0.5 LSB	1	1 0 0 0 0 0 0 0
	0	1 0 0 0 0 0 0 0
–1.5 LSB	0	1 0 0 0 0 0 0 0
	0	1 0 0 0 0 0 0 1
•	•	•
•	•	•
•	•	•
–1.0 V	0	1 1 0 0 0 0 0 0
	0	0 1 0 0 0 0 0 0
•	•	•
•	•	•
•	•	•
–2.0 V +0.5 LSB	0	0 0 0 0 0 0 0 1
	0	0 0 0 0 0 0 0 0
<(–2.0 V +0.5 LSB)	0	0 0 0 0 0 0 0 0

↻ Indicates the transition between the two codes

THERMAL MANAGEMENT

The typical thermal impedance is as follows:

ΘCA = +17 °C/W in still air with no heat sink

We highly recommend that a heat sink be used for this device with adequate air flow to ensure rated performance of the device. We have found that a Thermalloy 17846 heat sink with a minimum air flow of 1 meter/second (200 linear feet per minute) provides adequate thermal performance under laboratory tests. Application specific conditions should be taken into account to ensure that the device is properly heat sinked.

OPERATION

The SPT7750 has 256 preamp/comparator pairs which are each supplied with the voltage from V_{RT} to V_{RB} divided equally by the resistive ladder as shown in the block diagram. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at V_{IN} is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compare the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to V_{RT} (0 V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled ("track") when the clock changes from high to low. From here, the output of the latches are coded into 6 LSBs from 4 columns and 4 columns are coded into 2 MSBs. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

Figure 2 – Timing Diagram

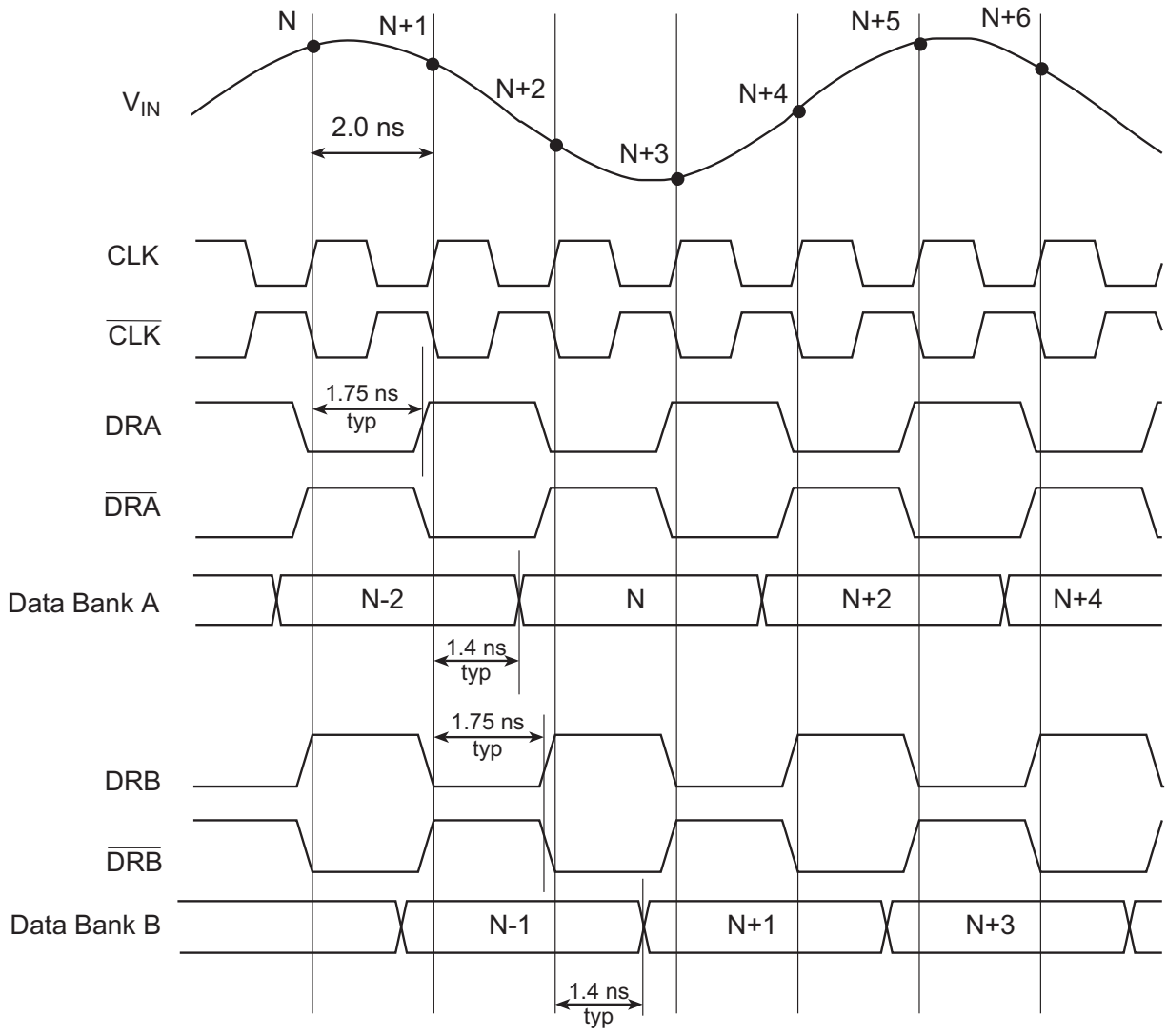
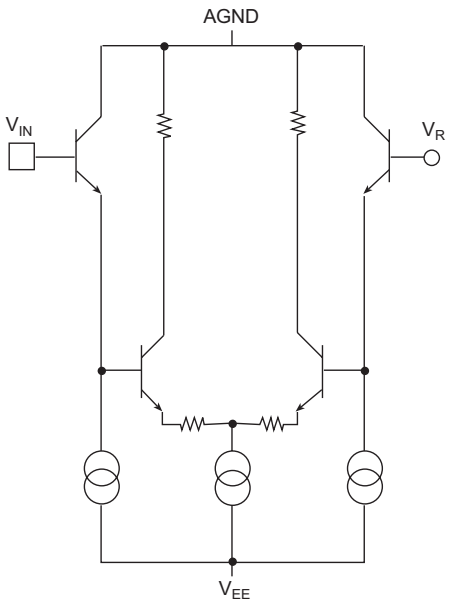
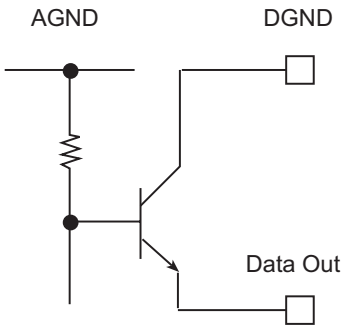


Figure 3 – Subcircuit Schematics

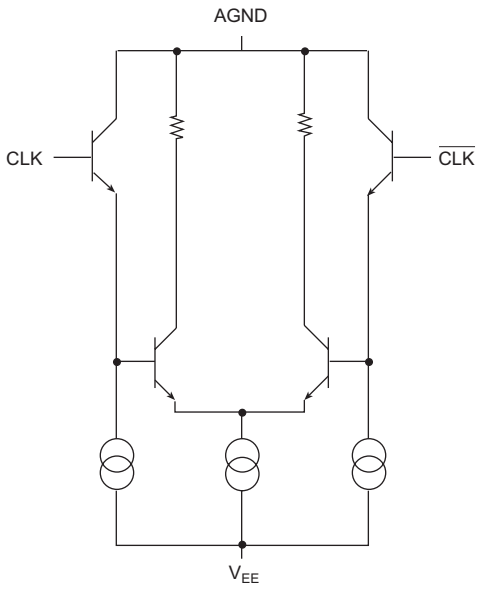
Input Circuit



Output Circuit

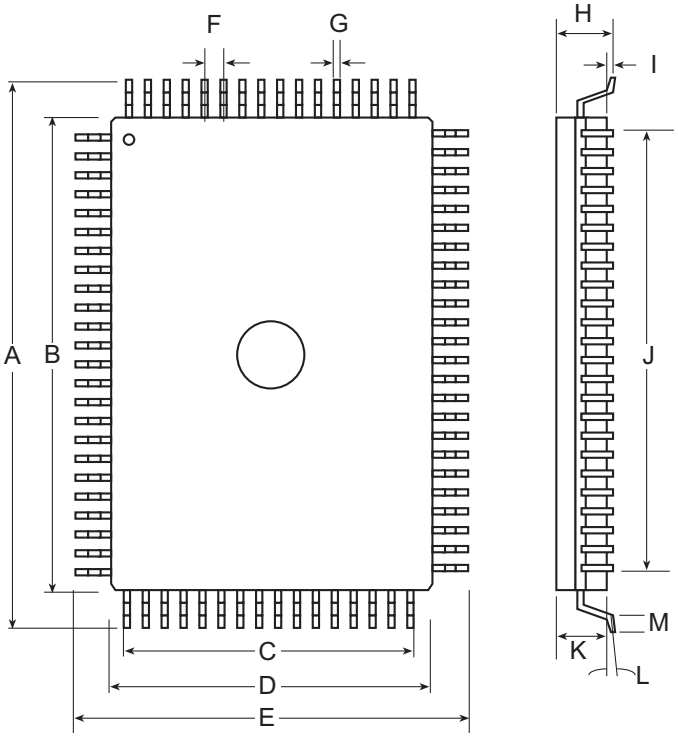


Clock Input



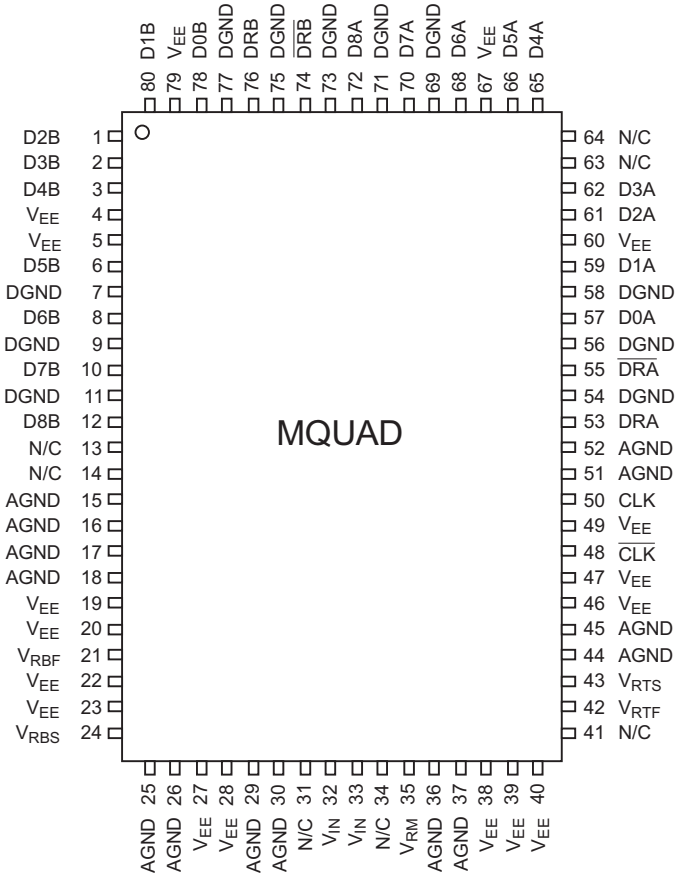
PACKAGE OUTLINE

80-Lead MQuad



	Inches		Millimeters	
Symbol	**Min**	**Max**	**Min**	**Max**
A	0.904	0.923	22.95	23.45
B	0.777	0.781	19.74	19.84
C	0.472 typ		12.00 typ	
D	0.541	0.545	13.74	13.84
E	0.667	0.687	16.95	17.45
F	0.031 typ		0.80 typ	
G	0.012	0.018	0.30	0.45
H	0.109	0.134	2.76	3.40
I	0.010	0.024	0.25	0.60
J	0.724 typ		18.40 typ	
K	0.099	0.110	2.51	2.80
L	0°	7°	0°	7°
M	0.029	0.041	0.73	1.03

PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
V_{EE}	Negative Supply Nominally –5.2 V
AGND	Analog Ground
V_{RTF}	Reference Voltage Force Top, Nominally 0 V
V_{RTS}	Reference Voltage Sense Top
V_{RM}	Reference Voltage Middle, Nominally –1 V
V_{RBF}	Reference Voltage Force Bottom, Nominally –2 V
V_{RBS}	Reference Voltage Sense Bottom
V_{IN}	Analog Input Voltage, Can Be Either Voltage or Sense
DGND	Digital Ground
D0–D7A	Data Output Bank A
D0–D7B	Data Output Bank B
DRA	Data Ready Bank A
$\overline{DRA}$	Not Data Ready Bank A
DRB	Data Ready Bank B
$\overline{DRB}$	Not Data Ready Bank B
D8A	Overrange Output Bank A
D8B	Overrange Output Bank B
CLK	Clock Input
$\overline{CLK}$	Clock Input

ORDERING INFORMATION

PART NUMBER	DESCRIPTION	TEMPERATURE RANGE	PACKAGE
SPT7750AIK	ILE = 1.0 LSB	–25 to +85 °C	80L MQUAD
SPT7750BIK	ILE = 1.5 LSB	–25 to +85 °C	80L MQUAD

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