FAIRCHILD
SEMICONDUCTOR®

SPT7720

8-BIT, 200 MSPS A/D CONVERTER

TECHNICAL DATA

MAY 9, 2001

FEATURES

- Pin-compatible with AD9054
- High conversion rate: 200 MSPS
- Less than ±1/2 LSB DLE
- 7.16 effective number of bits (ENOB) at 70 MHz
- Single +5 V power supply
- Internal THA and voltage reference
- Low power: 430 mW
- 500 MHz full-power bandwidth
- 1 V_{PP} input range
- Single or demuxed TTL output ports
- 44-lead TQFP

APPLICATIONS

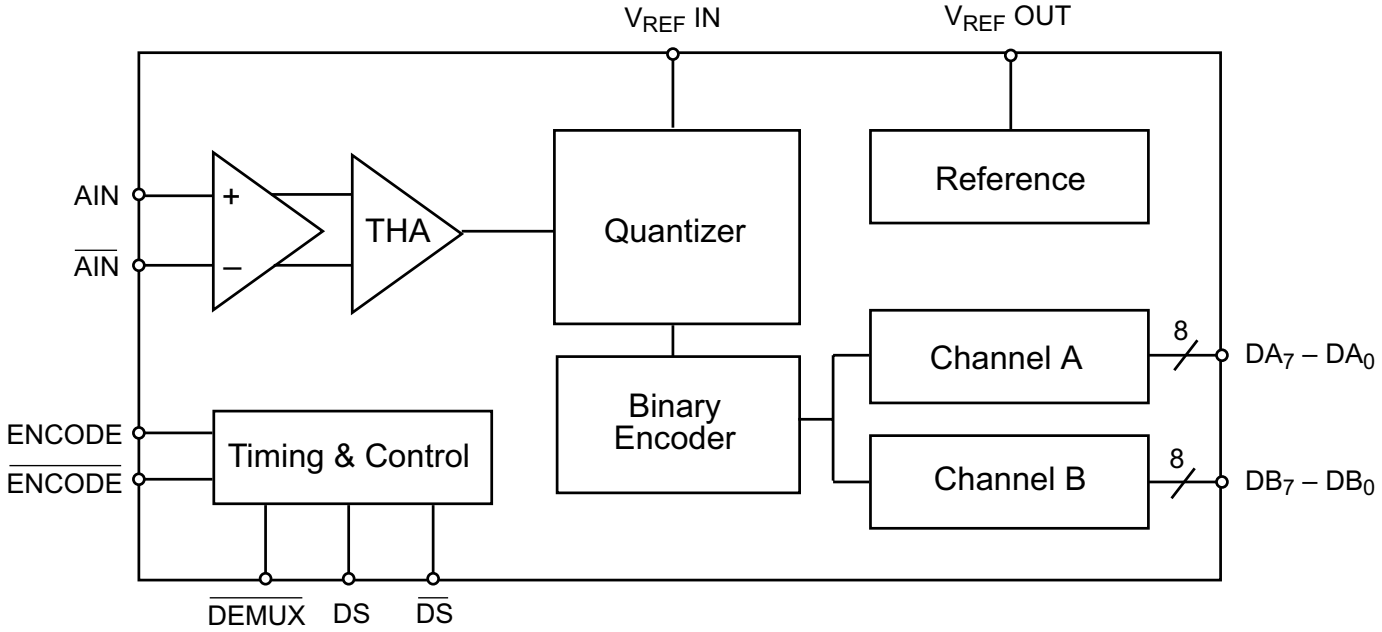
- Digital sampling oscilloscopes (DSO)
- RGB video processing
- Digital communications
- High-speed instrumentation
- Projection display systems

GENERAL DESCRIPTION

The SPT7720 is an 8-bit, high-speed, analog-to-digital converter implemented in a 0.5 µm BiCMOS process. It utilizes a folding and interpolating architecture that provides both high sample rates and low power. The device comes complete with a high bandwidth track-and-hold amplifier and internal voltage reference.

The SPT7720 digital inputs interface directly to TTL, CMOS or positive ECL (PECL) logic. The digital outputs are user selectable in either single-channel or dual-channel modes. It is a pin-compatible, direct replacement for the AD9054. The SPT7720 is available in a 44-lead TQFP surface mount package over the industrial temperature range of –40 to +85 °C.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{DD} ..... +6 V

Input Voltages

Analog Inputs ..... 0.0 to V_{DD}

Digital Inputs ..... 0.0 to V_{DD}

V_{REFL}, V_{REFH} ..... 0.0 to V_{DD}

Temperatures

Operating Temperature ..... –40 to +85 °C

Storage Temperature ..... –65 to +125 °C

Note 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{DD}=+5.0 V, external reference, f_S=200 MSPS, input amplitude = –1 dBFS, unless otherwise noted

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7720 MIN	SPT7720 TYP	SPT7720 MAX	UNITS
DC Accuracy						
Differential Linearity Error (DLE)	+25 °C	I		±0.41	±0.75	LSB
	–40 °C to +85 °C	V		±1.0	±1.0	LSB
Integral Linearity Error (ILE)	+25 °C	I		±0.56	±1.0	LSB
	–40 °C to +85 °C	V		±0.9	±1.2	LSB
No Missing Codes		VI		Guaranteed		
Gain Error	+25 °C	I		±1.06	±1.08	%FS
Gain Tempco		V		0		ppm/°C
Switching Performance						
Encode Pulsewidth High	+25 °C	IV	2.125	15		ns
Encode Pulsewidth Low	+25 °C	IV	2.125	15		ns
Aperture Delay (t_A)	+25 °C	V		0.57		ns
Aperture Uncertainty (Jitter) & Noise	+25 °C	V		4.5		ps rms
Data Sync Setup Time (t_{SDS})	+25 °C	IV	0			ns
Data Sync Hold Time (t_{HDS})	+25 °C	IV	0.5			ns
Data Sync Pulsewidth Time (t_{PWDS})	+25 °C	IV	2.0			ns
Output Valid Time (t_V)		IV	4.4	5.7		ns
Output Prop. Delay (t_{PD})		IV		6.7	8.0	ns
Dynamic Performance						
Transient Response	+25 °C	V		1.5		ns
Overvoltage Recovery Time	+25 °C	V		1.5		ns
Signal-to-Noise Ratio (SNR) (without harmonics)						
f_{IN} = 19.7 MHz	+25 °C	V		47		dB
f_{IN} = 19.7 MHz	–40 °C to +85 °C	V		47		dB
f_{IN} = 70.1 MHz	+25 °C	I	44	46.3		dB
f_{IN} = 70.1 MHz	–40 °C to +85 °C	V		45.8		dB
Signal-to-Noise Ratio and Distortion (SINAD)						
f_{IN} = 19.7 MHz	+25 °C	V		47		dB
f_{IN} = 19.7 MHz	–40 °C to +85 °C	V		43		dB
f_{IN} = 70.1 MHz	+25 °C	I	43	44.9		dB
f_{IN} = 70.1 MHz	–40 °C to +85 °C	V		44.5		dB
2nd Harmonic Distortion						
f_{IN} = 19.7 MHz	+25 °C	V		–59		dBc
f_{IN} = 70.1 MHz	+25 °C	V		–55.4		dBc
3rd Harmonic Distortion						
f_{IN} = 19.7 MHz	+25 °C	V		–58		dBc
f_{IN} = 70.1 MHz	+25 °C	V		–56.4		dBc
Total Harmonic Distortion (THD)						
f_{IN} = 70.1 MHz	+25 °C	I		–50.9	–46.0	dBc
f_{IN} = 70.1 MHz	–40 to +85 °C	V		–48.3		dBc
Effective Number of Bits (ENOB)						
f_{IN} = 70.1 MHz	+25 °C	I	6.9	7.16		Bits
f_{IN} = 70.1 MHz	–40 to +85 °C	V	6.5			Bits

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{DD}=+5.0 V, external reference, f_S=200 MSPS, input amplitude = –1 dBFS, unless otherwise noted

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7720 MIN	SPT7720 TYP	SPT7720 MAX	UNITS
Analog Input						
Input Voltage Range (differential)		V		±0.5		V
Compliance Range		V	1.8		3.2	V
Input Offset Voltage	+25 °C	I		±4	±16	mV
Input Offset Voltage	–40 °C to +85 °C	V		±8	±19	mV
Input Resistance	+25 °C	V	36	62		kΩ
Input Capacitance		V		4		pF
Input Bias Current	+25 °C	I		11	50	µA
Input Bias Current	–40 °C to +85 °C	V			75	µA
Full Power Bandwidth		V		500		MHz
Reference Output Voltage		VI	2.4	2.5	2.6	V
Temperature Coefficient		V		110		ppm/°C
Differential Digital Inputs						
High Level Current	–40 to +85 °C >1.5 V differential	V		500	625	µA
Low Level Current	–40 to +85 °C >1.5 V differential	V		500	625	µA
Input Capacitance		V		3		pF
Differential Inputs						
Differential Signal Amplitude		IV	400			mV
High Input Voltage		IV	1.5		V_{DD}	V
Low Input Voltage		IV	0		V_{DD}–0.4	V
Common-Mode Input Voltage		IV	1.5			V
Demux Input						
High Input Voltage		VI	2.0		V_{DD}	V
Low Input Voltage		VI	0		0.8	V
Digital Outputs						
High Output Voltage	Source 800 µA	VI	2.4	3.9		V
Low Output Voltage	Sink 1.6 mA	VI		0.8	0.4	V
Output Coding				Binary		
Power Supply						
V_{DD} Supply Current	–40 to +85 °C	VI		86	111	mA
Power Dissipation		VI		430	555	mW
Power Supply Sensitivity	+25 °C	IV		0.005	0.015	V/V

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 – Timing Diagram – Single-Channel Mode

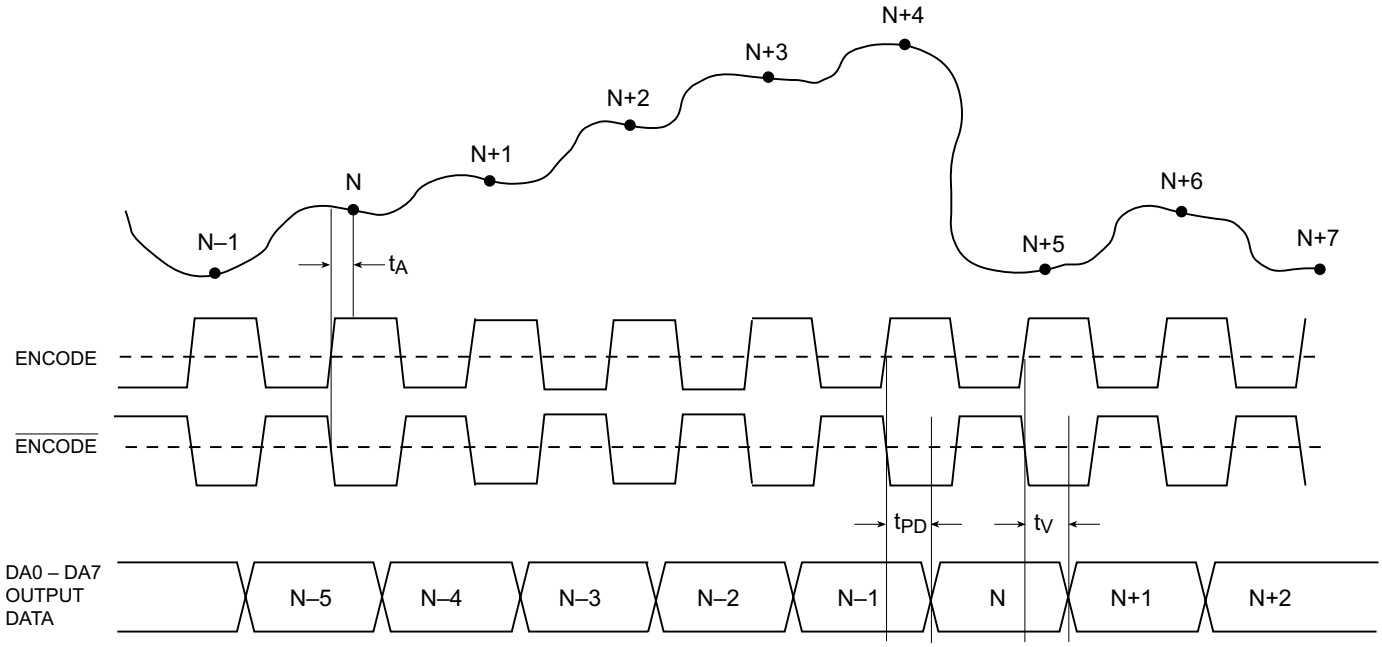
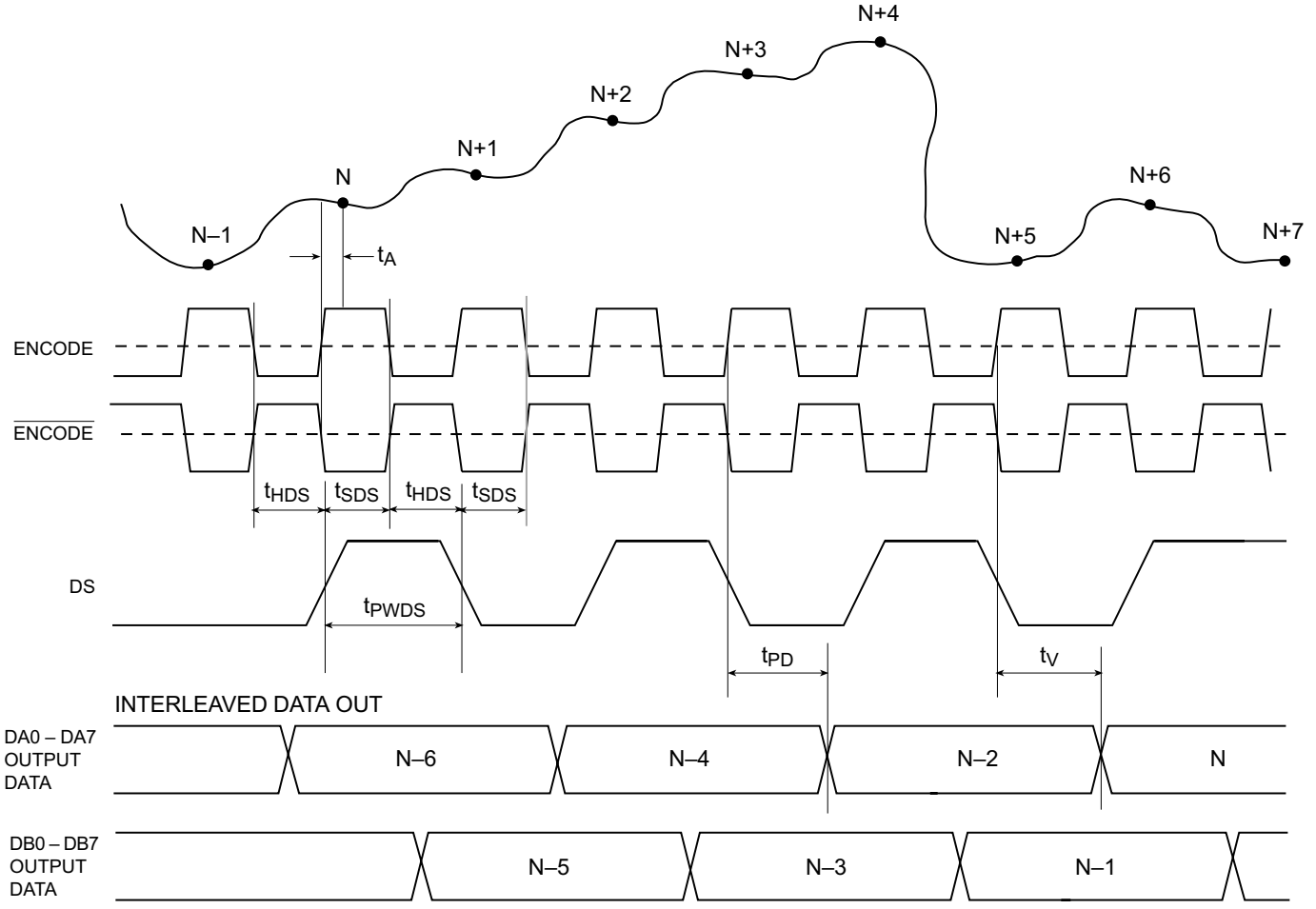
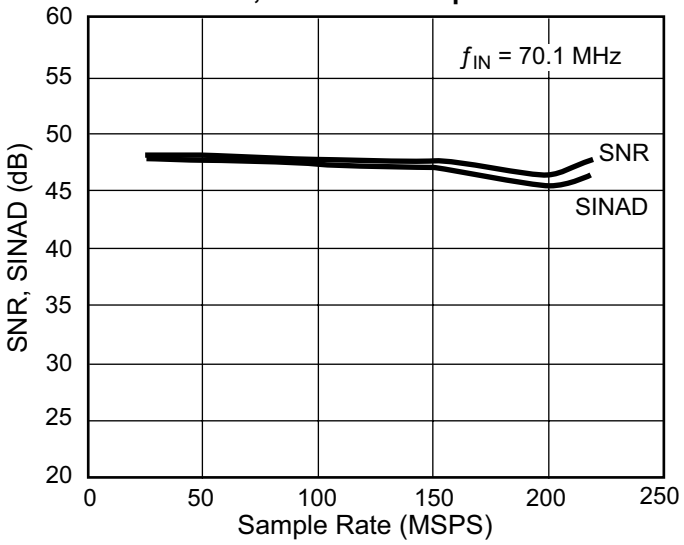


Figure 2 – Timing Diagram – Dual-Channel Mode

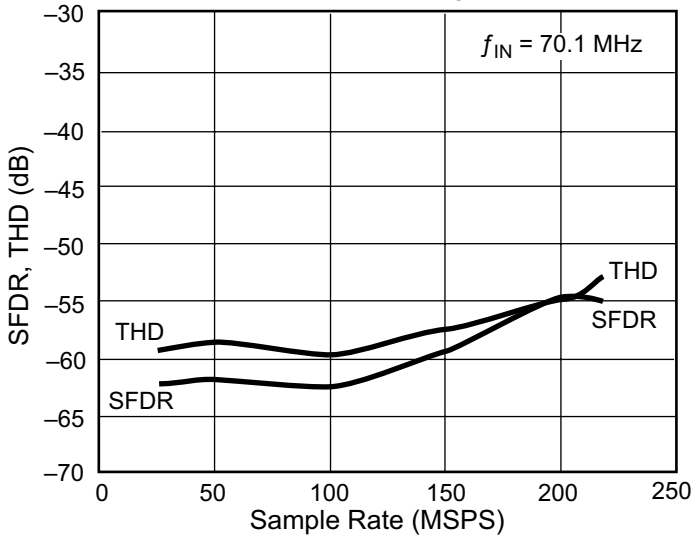


TYPICAL PERFORMANCE CHARACTERISTICS

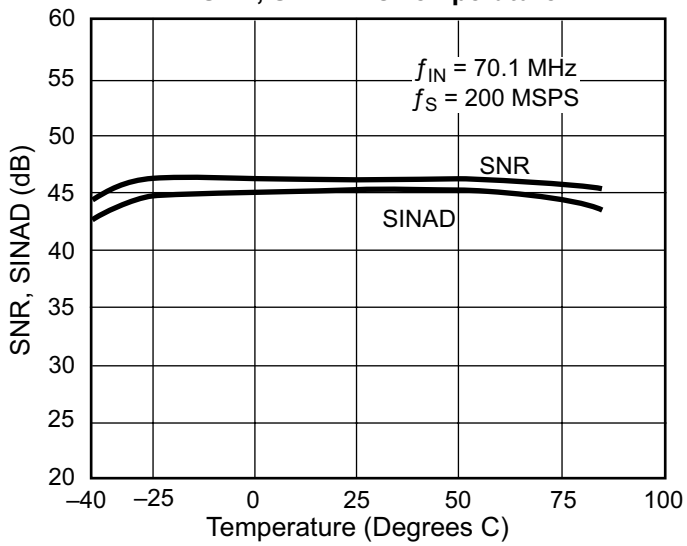
SNR, SINAD vs Sample Rate



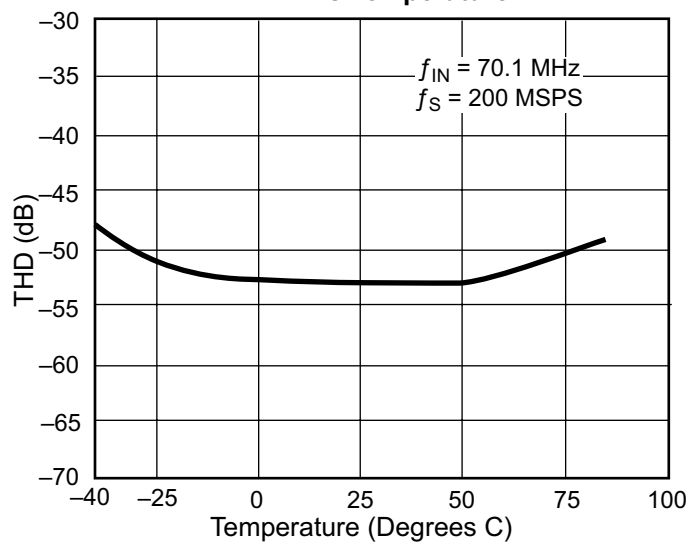
SFDR, THD vs Sample Rate



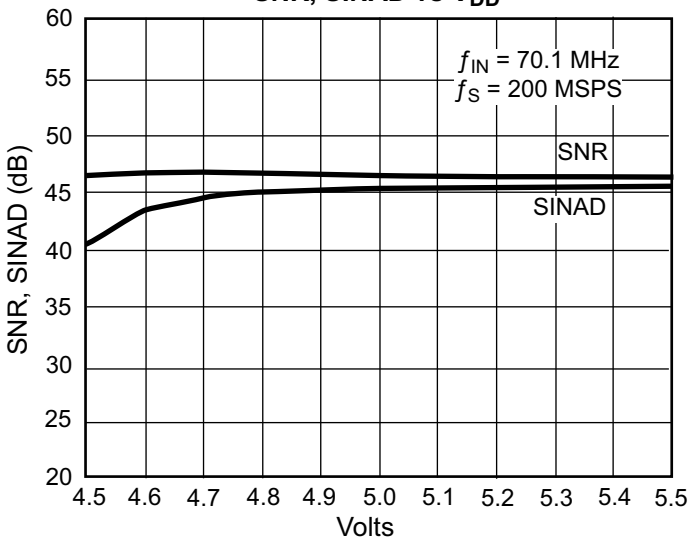
SNR, SINAD vs Temperature



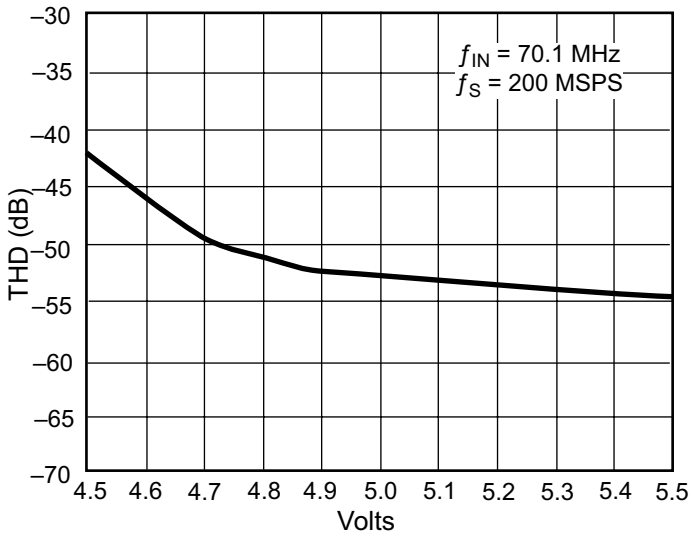
THD vs Temperature



SNR, SINAD vs V_{DD}

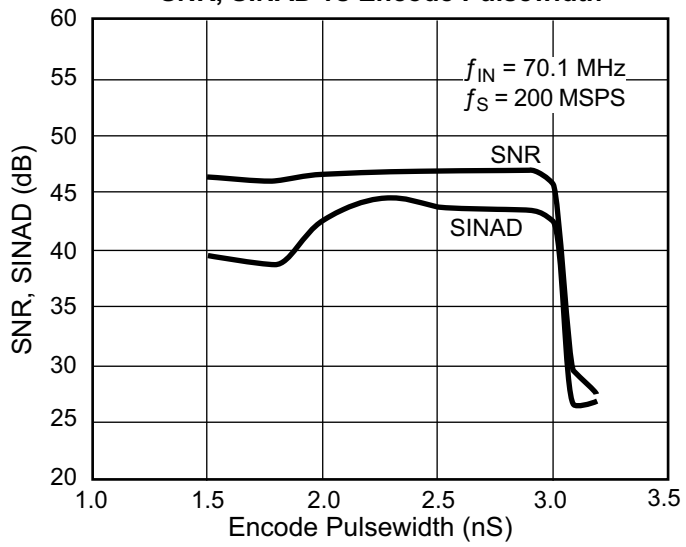


THD vs V_{DD}

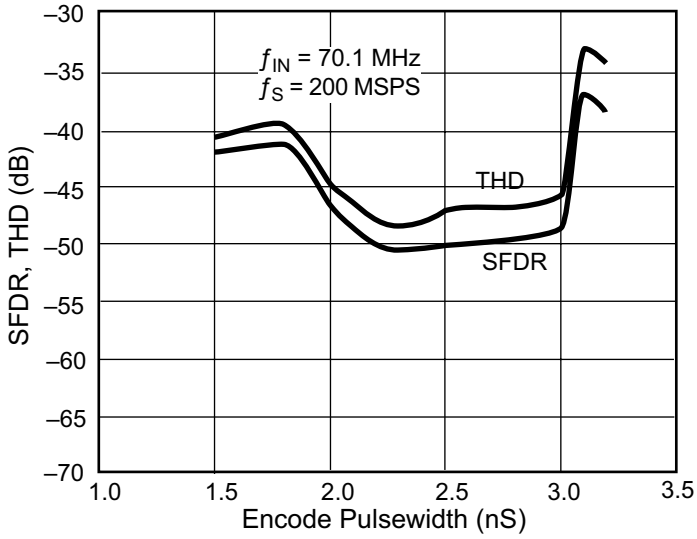


TYPICAL PERFORMANCE CHARACTERISTICS

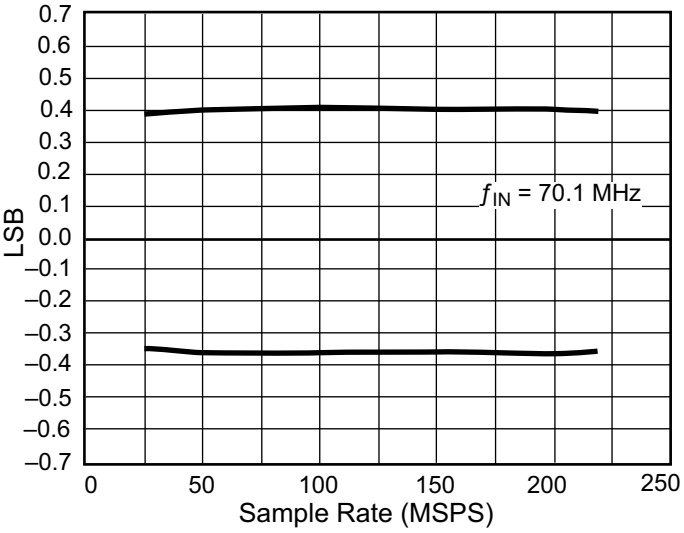
SNR, SINAD vs Encode Pulsewidth



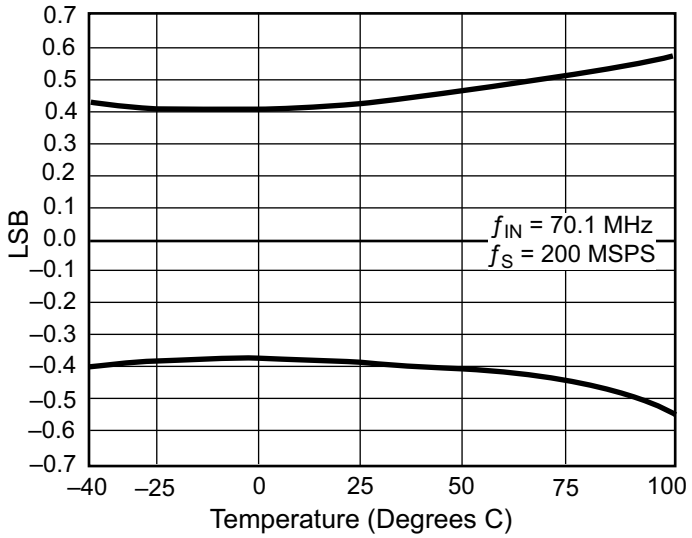
SFDR, THD vs Encode Pulsewidth



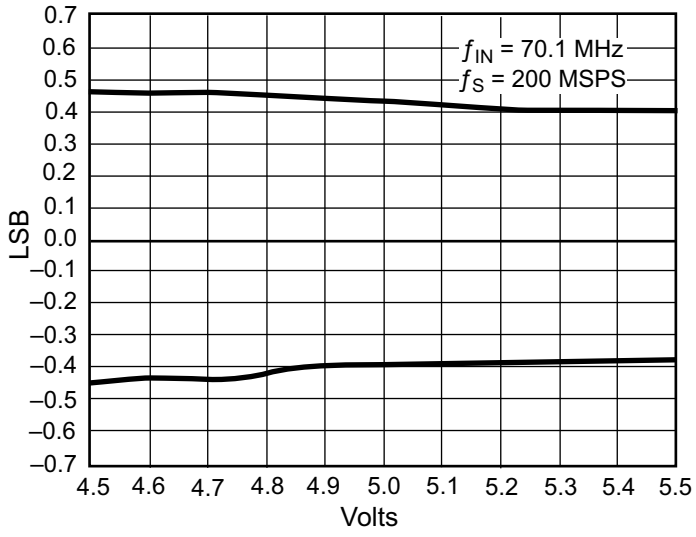
DLE vs Sample Rate



DLE vs Temperature



DLE vs V_{DD}



Supply Current vs Temperature

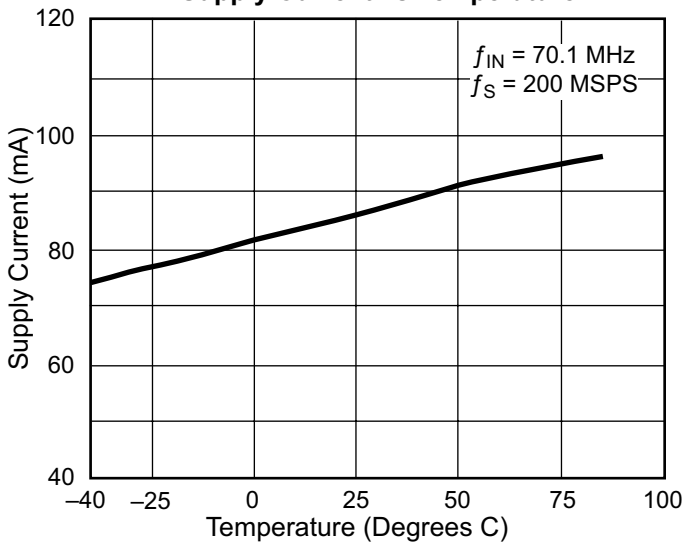
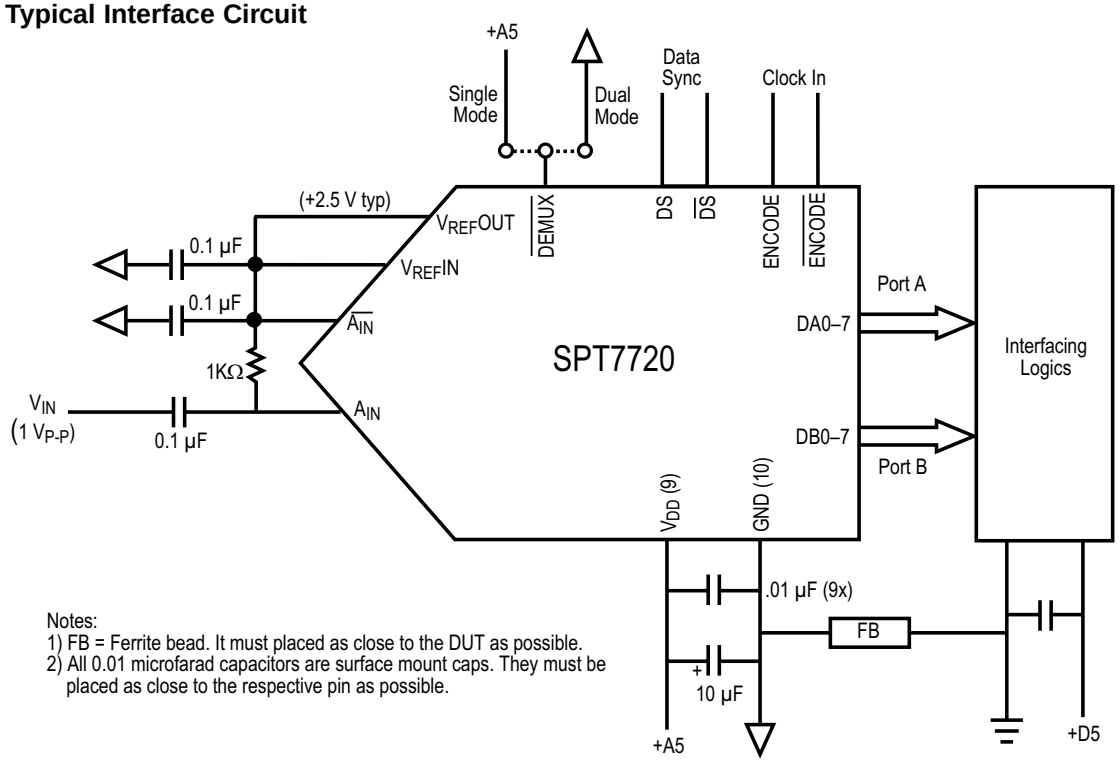


Figure 3 – Typical Interface Circuit



TYPICAL INTERFACE CIRCUIT

Very few external components are required to achieve the stated device performance. Figure 3 shows the typical interface requirements when using the SPT7720 in normal circuit operation. The following sections provide descriptions of the major functions and outline performance criteria to consider for achieving the optimal device performance.

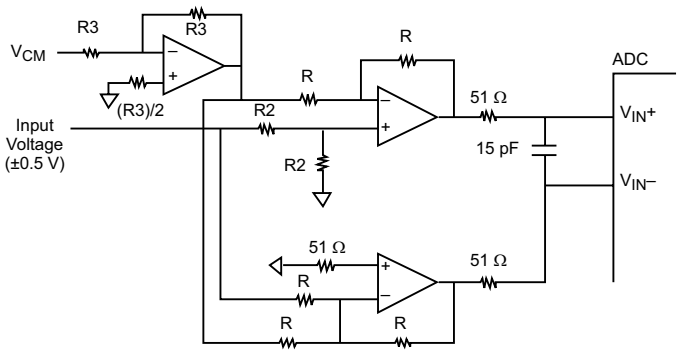
ANALOG INPUT

The input of the SPT7720 can be configured in various ways depending on whether a single-ended or differential input is desired.

The AC-coupled input is most conveniently implemented using a transformer with a center-tapped secondary winding. The center tap is connected to the V_{CM} pin as shown in figure 3. To obtain low distortion, it is important that the selected transformer does not exhibit core saturation at the full-scale voltage. Proper termination of the input is important for input signal purity. A small capacitor across the input attenuates kickback noise from the internal track-and-hold.

Figure 4 illustrates a solution (based on operational amplifiers) that can be used if a DC-coupled single-ended input is desired. It is very important to select op amps with a high open-loop gain, a bandwidth high enough so as not to impair the performance of the ADC, low THD, and high SNR.

Figure 4 – DC-Coupled Single-Ended to Differential Conversion (power supplies and bypassing are not shown)



INPUT PROTECTION

All I/O pads are protected with an on-chip protection circuit. This circuit provides ESD robustness and prevents latchup under severe discharge conditions without degrading analog transmission times.

POWER SUPPLIES AND GROUNDING

The SPT7720 is operated from a single power supply in the range of 4.75 to 5.25 volts. Normal operation is suggested to be 5.0 volts. All power supply pins should be bypassed as close to the package as possible.

REFERENCES

To save on parts count, design time, and PC board real estate, the SPT7720 utilizes an internal reference. No other external components are required to implement this feature.

VOLTAGE REFERENCE CIRCUIT

The SPT7720 has an on-board voltage reference circuit (V_{REF}). It is 2.5 volts and is capable of driving 50 µA loads typically. The circuit is commonly used to drive the center tap of the RF transformer in fully differential applications. For single-ended applications, this output can be used to provide the level shifting required for the single-to-differential converter conversion circuit.

ENCODE INPUT

The ENCODE input on the SPT7720 can be driven by either a single-ended or differential clock circuit and can handle TTL, PECL, and CMOS signals. When operating at high sample rates it is important to keep the pulse width of the duty signal as close to 50% as possible. For TTL/CMOS single-ended ENCODE inputs, the rise time of the signal also becomes an important consideration. The ENCODE input is 300 Ω into a bipolar differential pair. $\overline{\text{ENCODE}}$ is internally biased to 1.5 V with a Thevenin equivalent of 5.25 kΩ.

DIGITAL INPUTS

The DS input is 35 Ω into one side of a differential pair. There is a two-diode clamp from DS to $\overline{\text{DS}}$ in both directions. $\overline{\text{DS}}$ is biased to 1.5 V with a Thevenin equivalent of 5.25 kΩ.

The $\overline{\text{DEMUX}}$ pin is input to one side of a CMOS differential pair. The other side is internally biased to 1.5 V and does not connect to the outside.

DIGITAL OUTPUTS

The output circuitry of the SPT7720 has been designed to be able to support two separate output modes. The demuxed (double-wide) mode supports interleaved data output. The single-channel mode is not demuxed and can support direct output at speeds up to 100 MSPS.

The output format is straight binary (table I).

Table I – Output Data Format

Analog Input	Output Code D7–D0
+FS	1111 1111
+FS – 1/2 LSB	1111 111Ø
+1/2 FS	ØØØØ ØØØØ
–FS + 1/2 LSB	0000 000Ø
–FS	0000 0000

Ø indicates the flickering bit between logic 0 and 1

The data output mode is set using the $\overline{\text{DEMUX}}$ input (pin 42). Table II describes the mode switching options.

Table II – Output Data Modes

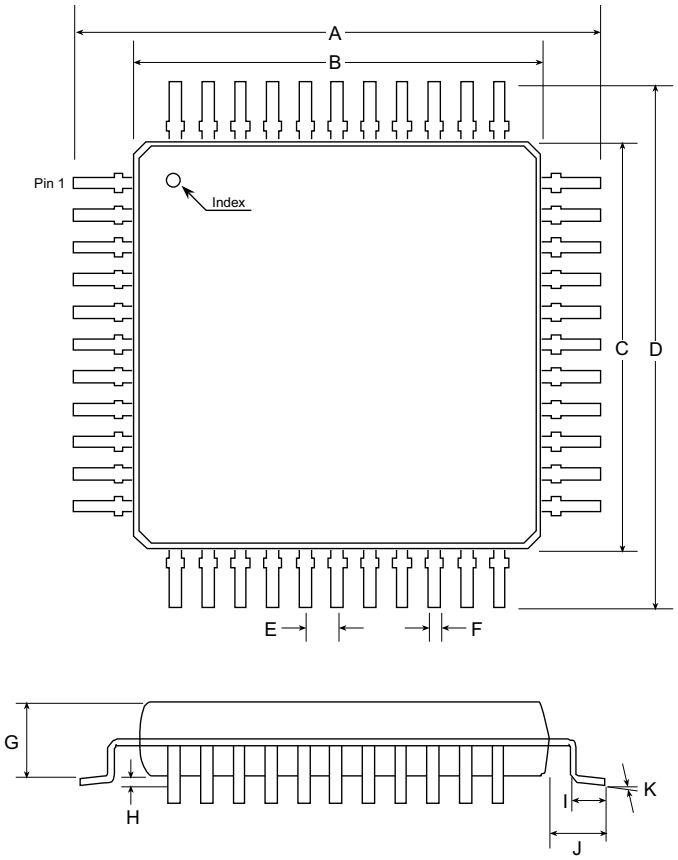
Output Mode	$\overline{\text{DEMUX}}$
Interleaved Dual Channel Output	0
Single Channel Data Output (Bank A only 100 MSPS max)	1

EVALUATION BOARD

The EB7720 evaluation board is available to aid designers in demonstrating the full performance of the SPT7720. This board includes a clock driver and reset circuit, adjustable references and common mode, a single-ended to differential input buffer and a single-ended to differential transformer (1:1). An application note (AN7720) describing the operation of this board, as well as information on the testing of the SPT7720, is also available. Contact the factory for price and availability of the EB7720.

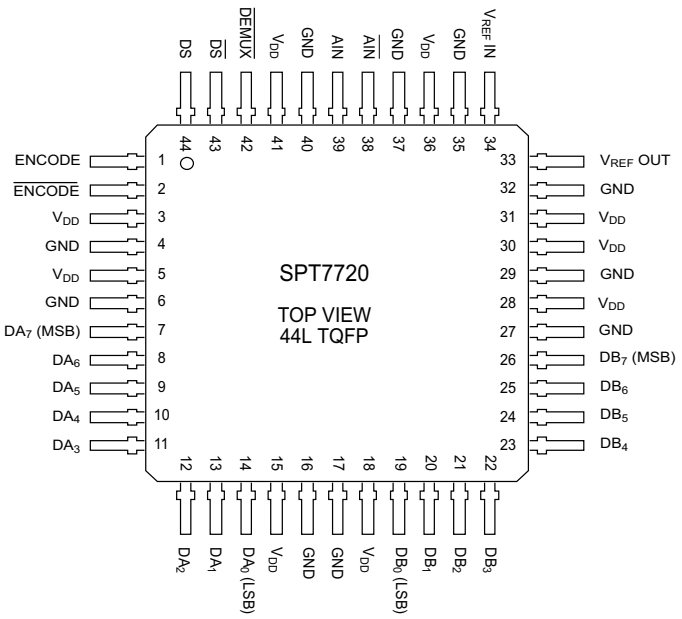
PACKAGE OUTLINE

44-Lead TQFP



	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.472 Typ		12.00 Typ	
B	0.394 Typ		10.00 Typ	
C	0.394 Typ		10.00 Typ	
D	0.472 Typ		12.00 Typ	
E	0.031 Typ		0.80 Typ	
F	0.012	0.018	0.300	0.45
G	0.053	0.057	1.35	1.45
H	0.002	0.006	0.05	0.15
I	0.018	0.030	0.450	0.750
J	0.039 Typ		1.00 Typ	
K	0-7°		0-7°	

PIN ASSIGNMENTS



PIN FUNCTIONS

Pin Name	Description
AIN, $\overline{AIN}$	Differential Input Pins
ENCODE $\overline{ENCODE}$	Differential Clock Input
V_{DD}	Power Supply
GND	Ground
DA_0–DA_7	Digital Outputs, Channel A
DB_0–DB_7	Digital Outputs, Channel B
V_{REF} OUT	Reference Output Voltage
V_{REF} IN	Reference Input Voltage, High
$\overline{DEMUX}$	Format Select: LOW = Dual-Channel Mode, HIGH = Single-Channel Mode
DS, $\overline{DS}$	Data Sync and Data Sync Complement – Aligns Output Channels in Dual-Channel Mode

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SPT7720SIT	–40 to +85 °C	44L TQFP

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.