SPT5220

10-BIT, 80 MWPS VIDEO DAC

FEATURES

- 80 MWPS Pipelined Operation
- +5 V CMOS Monolithic Construction
- ±0.4 LSB Differential Linearity Error
- ±0.6 LSB Integral Linearity Error
- TTL-Compatible Inputs
- RS-343A/RS-170 Compatible Outputs
- Binary or Two's Complement Input Data Format
- Low Power Dissipation of 260 mW
- Internal/External Voltage Reference

APPLICATIONS

- High Resolution Color Graphics
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- General Purpose High-Speed D/A Conversion
- Direct Digital Synthesis (DDS)
- Digital Radio Transmitters/Modulators
- High Definition Television (HDTV)

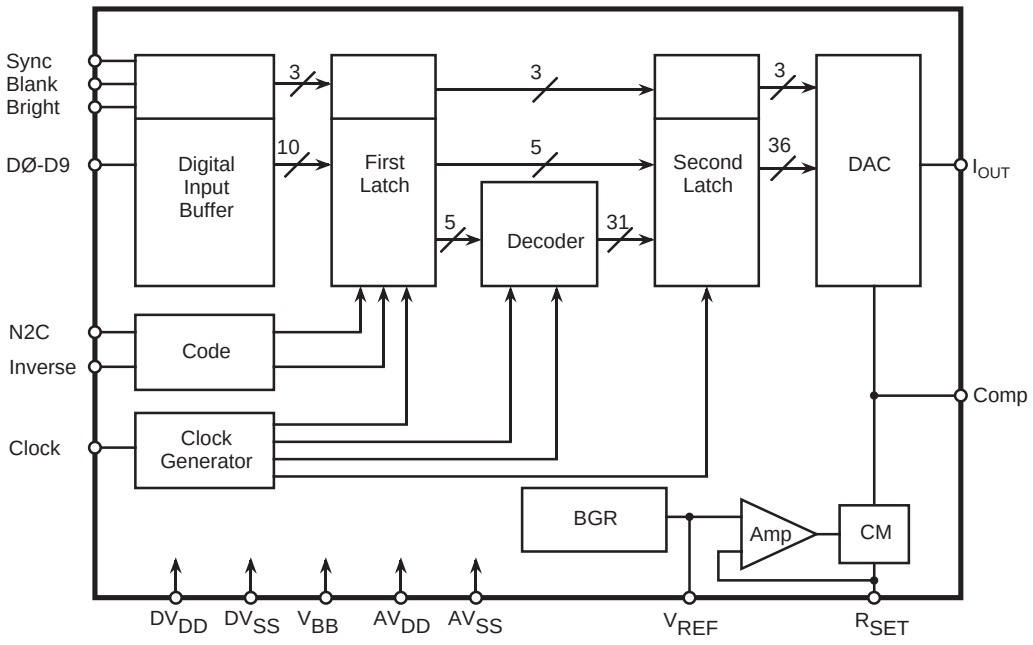
GENERAL DESCRIPTION

The SPT5220 is a monolithic 10-bit, 80 MWPS CMOS D/A converter for high-resolution color graphics and video system applications. The device operates from a single +5 V power supply and all digital inputs are TTL/CMOS compatible.

The SPT5220 generates RS343A-compatible video outputs (capable of driving a doubly-terminated 75 Ω load) and RS170-compatible video outputs (capable of driving a singly-terminated 75 Ω load) without the need for external buffers. The data latches minimize the data time skew and reduce the glitches that can adversely affect many applications.

The device is available in a 28-lead plastic DIP package over the commercial temperature range.

BLOCK DIAGRAM



Signal Processing Technologies, Inc.

4755 Forge Road, Colorado Springs, Colorado 80907, USA

Phone: (719) 528-2300 FAX: (719) 528-2370

ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1,2,3]

Supply Voltages

AV_{DD} ..... -0.5 to +7.0 V
DV_{DD} ..... -0.5 to +7.0 V

Input Voltages

Any Digital Pin ..... DV_{SS}-3.0 V to DV_{DD}+3.0 V

ESD Susceptibility ..... ±2,000 V

Temperature

Operating Temperature Range (Ambient) ..... 0 to +70 °C
Storage Temperature ..... -55 to +150 °C

Notes: 1. Operation at any absolute maximum rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.
2. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is not implied.
3. Applied voltage must be current limited to the specified range.

ELECTRICAL SPECIFICATIONS[4]

$T_A=T_{MIN}$ to T_{MAX}, $AV_{DD}=DV_{DD}=V_{BB}$=+5.0 V, $AV_{SS}=DV_{SS}$=0.0 V, V_{REF}=1.235 V, R_{SET}=165 Ω, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT5220 MIN	SPT5220 TYP	SPT5220 MAX	UNITS
DC CHARACTERISTICS						
Resolution			10			Bits
Differential Linearity Error		VI		±0.4	±1.0	LSB
Integral Linearity Error		VI		±0.6	±1.0	LSB
Gray Scale Error		VI			±5.0	% Gray
Monotonicity		VI		Guaranteed		
Digital Input High Current	V_{IN}=2.4 V	VI			1.0	µA
Digital Input Low Current	V_{IN}=0.4 V	VI	-1.0			µA
Digitial Input Capacitance	f_{IN}=1 MHz	IV		20	40	pF
Analog Outputs						
Gray Scale Current		VI			22	mA
Output Current						
	Bright to White	VI	1.0	1.90	3.0	mA
	White to Black	VI	18.1	19.05	20.0	mA
	Black to Blank	VI	0.5	1.43	2.5	mA
	Blank to Sync	VI	6.5	7.62	8.5	mA
	Sync Level	VI	0	5	50	µA
	LSB Size	V		18.62		µA
Output Compliance		VI	-1.0		+1.5	V
Output Impedence		V		11		kΩ
Output Capacitance	f_{IN}=1 MHz	IV		14	30	pF
Internal Reference Voltage		VI	1.16	1.235	1.36	V
Power Supply Rejection Ratio	f_{IN}=1 kHz, comp=0.1 µF	V		-30		dB
Operating Supply Voltage		VI	4.75	5.00	5.25	V
Digital Input Voltage	High	VI	2.0		V_{DD}+0.3	V
	Low	VI	V_{SS}-0.3		0.8	V
Effective Output Load		V		37.5		Ω
Data Input Setup Time		IV	2.0			ns
Data Input Hold Time		IV	2.0			ns
Clock Cycle Time		IV	12.5			ns
Clock Pulse Width High		IV	5			ns
Clock Pulse Width Low		IV	5			ns

Note: 4. To avoid power latch-up, drive all supply pins (AV_{DD}, DV_{DD}, and V_{BB}) from the same source.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, $AV_{DD}=DV_{DD}=V_{BB}$=+5.0 V, $AV_{SS}=DV_{SS}$=0.0 V, V_{REF}=1.235 V, R_{SET}=165 Ω, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT5220 MIN	SPT5220 TYP	SPT5220 MAX	UNITS
AC CHARACTERISTICS						
Clock Rate			80			MWPS
Analog Output Delay		V		7		ns
Analog Output Rise Time		V		4		ns
Analog Output Fall Time		V		4		ns
Analog Output Settling Time[5]						
to ±1 LSB		IV		100	150	ns
to ±2 LSB		IV		70	100	ns
Clock and Data Feedthrough[5]		V		-34		dB
Glitch Impulse[5]		IV		30		pv-sec
Differential Gain Error		V		0.8		%
Differential Phase Error		V		0.9		Degree
Pipeline Delay (Clock Latency)		IV			1	Clock Cycles
V_{DD} Supply Current[6]		VI		50	70	mA

Note: 5. Clock and data feedthrough are functions of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough.

6. At f_{MAX}, IDD (typ) at $AV_{DD}=DV_{DD}$=5.25 V, CLK=0 V to 3 V (80 MWPS), NC2=High, Data (DØ-D9)=0 V to 3 V (40 MWPS), Inverse=Sync=Blank=Bright=Low.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=+25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

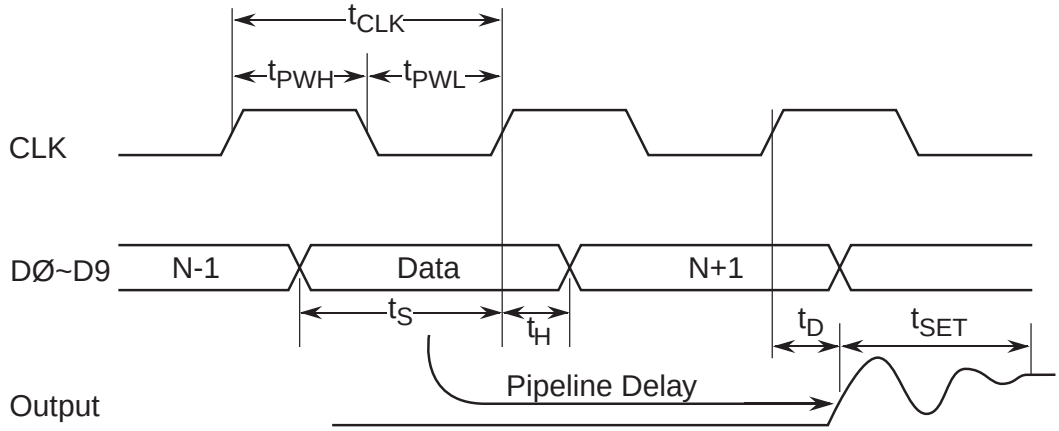
CIRCUIT DESCRIPTION AND OPERATION

The SPT5220 contains a 10-bit DAC, input buffers and latches, internally or externally generated voltage reference and complete video controls. The following describes the main operation of the device and outlines several considerations that should be noted to achieve the best performance.

CLOCK INPUT

CLK is the device clock input and is typically the pixel clock rate of the system. It is TTL compatible. The digital data D0-D9 and all video controls (SYNC, BLANK, BRIGHT) are all latched on the rising edge of CLK. See figure 1.

Figure 1: Timing Waveform[7,8,9]



Note:
7. Output delay (t_d) is measured from the 50% point of the rising edge of CLK to the full scale transition.
8. Settling time (t_{set}) is measured from the 50% point of full scale transition to the output remaining within ±1, ±2 LSB.
9. Output rise/fall time (t_r, t_f) is measured between the 10% and 90% points of full scale transition.

DIGITAL INPUTS AND VIDEO CONTROLS

All ten bits of data (D0-D9, D0 is the LSB) are latched into the device on the rising edge of each clock cycle. There are also three video control inputs to generate composite video outputs. They are SYNC, BLANK and BRIGHT. A logic 1 on the SYNC input generates the sync level. A logic 1 on the BLANK input generates the pedestal level. BRIGHT is the bright signal input. These inputs are pipelined to maintain synchronization with the digital input data. These video controls produce the output levels needed to be compatible with video system standards. Table I shows the video control effects on the analog output.

Table I - Video Output Truth Table

Sync	Blank	Bright	Data (D9-D0)	I_{OUT} (mA)	V_{OUT} (V)	Out (IRE)	Description
1	X	X	X	0	0	-40	Sync Level
0	1	X	X	7.62	0.286	0	Blank Level
0	0	0	000…	9.05	0.340	7.5	Black Level
0	0	0	111…	28.10	1.054	100	White Level
0	0	1	000…	10.95	0.410	17.5	Enhanced Black Level
0	0	1	111…	30.00	1.125	110	Enhanced White Level

Note: 10. Double-terminated load of 75 Ω. VREF=1.235 V R_{SET}=165 Ω. Inverse = 0. N2C = 1.

There are two different input data formats available: binary and two's complement. In addition, these formats can be either normal or inverted. The video control truth table for these options are given in table II.

Table II - Video Control Truth Table[11]

N2C	INVERSE	DATA (D9-D0)	OUTPUT (I/O)	DESCRIPTION
1	0	0000000000 1111111111	Black Level White Level	Binary
1	1	0000000000 1111111111	White Level Black Level	Inverse Binary
0	0	1000000000 0111111111	Black Level White Level	Two's Complement
0	1	1000000000 0111111111	White Level Black Level	Inverse Two's Complement

Note: 11. Doubly-terminated load of 75 Ω, Sync=Blank=Bright=Low

REFERENCE

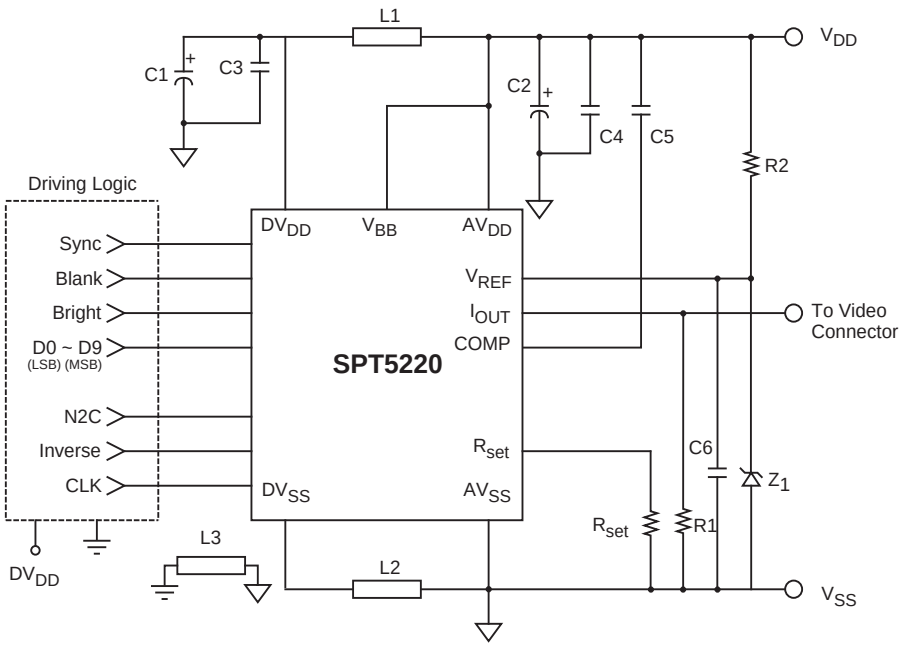
The SPT5220 can be used with either an internal or external voltage reference. The typical interface circuits are shown in figures 2 and 3. When using an external reference (figure 2), the input voltage supplied must be 1.235 volt (typ). When using the internal reference (figure 3), the V_{REF} pin should not drive any external circuitry except for the decoupling capacitor. A bypass capacitor of 0.1 µF with the shortest possible lead lengths should be connected between V_{REF} and V_{SS}. With either configuration, the COMP pin (compensation capacitor) should be connected to V_{DD} through the bypass capacitor. The COMP capacitor should be kept as close as possible to the device to keep the lead lengths to an absolute minimum.

Rset is the full scale adjust control. A resistor (Rset) connected between this pin and ground controls the magnitude of the full-scale video signal. The value for Rset is determined by the relationship:

$$Rset = 4.1 \times V_{REF}/I_{OUT}.$$

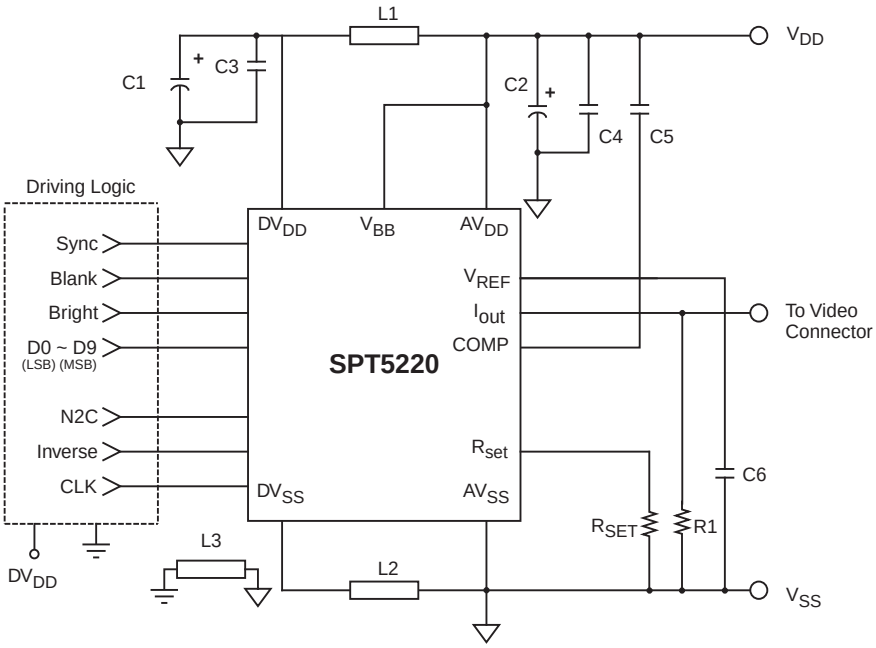
The electrical specifications are given with an Rset value of 165 ohms.

Figure 2 - Typical Interface Circuit (External Reference)



Component	Description
C1, C2	10 µF Capacitor
C3 - C6	0.1 µF Ceramic Capacitor
L1, L2, L3	Ferrite Bead
R1	75 Ω 1% Metal Film Resistor
R2	1 kΩ 5% Resistor
R_{SET}	165 Ω 1% Film Resistor (180 Ω//2 kΩ)
Z_1	1.235 V Voltage Reference (ICL8069CCSQ2)

Figure 3 - Typical Interface Circuit (Internal Reference)



Component	Description
C1, C2	10 µF Capacitor
C3 - C6	0.1 µF Ceramic Capacitor
L1, L2, L3	Ferrite Bead
R1	75 Ω 1% Metal Film Resistor
R_{SET}	165 Ω 1% Film Resistor (180 Ω//2 kΩ)

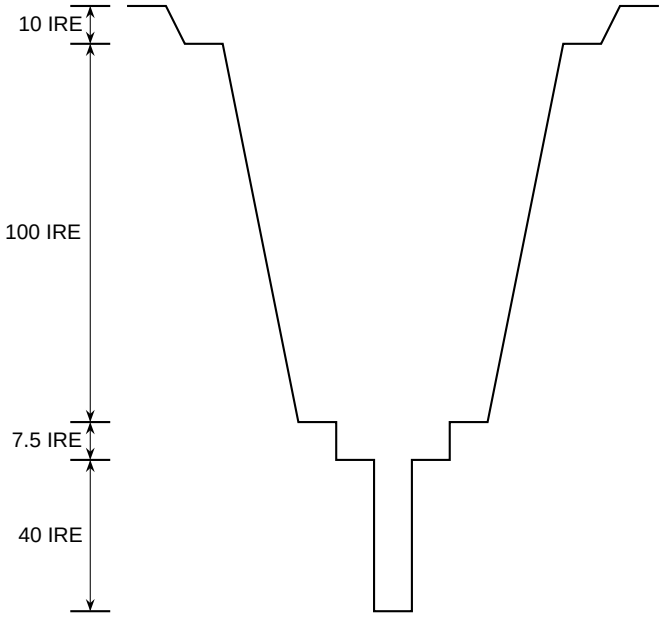
Note 12: AV_{DD}, DV_{DD} and V_{RB} must be supplied from the same source (Analog +5 V) to prevent a latch-up condition due to power supply sequencing.
Note 13: For applications requiring minimal signal distortion, use of the external reference is recommended.

ANALOG OUTPUT

The SPT5220 generates RS-343A compatible video outputs capable of directly driving a doubly-terminated 75 ohm load, and RS-170 compatible video outputs capable of directly driving a singly-terminated 75 ohm load without the need for external buffers. Figure 4 shows the video waveforms associated with the output driving the doubly-terminated 75 ohm load.

Figure 4 - Composite Video Output Wave Form[14]

LEVEL	mA	V
Bright	30.00	1.125
White	28.10	1.054
Black	9.05	0.340
Blank	7.62	0.286
Sync	0.00	0.00



Note: 14. Doubly-terminated load of 75 Ω, V_{REF}=1.235 V, R_{SET}=165 Ω. RS-343 levels and tolerances are assumed on all levels.

PC BOARD CONSIDERATIONS

LAYOUT CONSIDERATIONS

To minimize noise on the power lines and ground lines, shield and decouple the digital inputs. Keep the trace length between groups of V_{DD} (AV_{DD}, DV_{DD}) and V_{SS} (AV_{SS}, DV_{SS}) as short as possible to minimize inductive ringing.

SUPPLY AND GROUND CONSIDERATIONS

Use a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor for decoupling between the power line and the ground line. The digital power plane (DV_{DD}) and the analog power plane (AV_{DD}) are connected through a ferrite bead. The digital ground plane (DV_{SS}) and the analog ground plane (AV_{SS}) are also connected through a ferrite bead. (See figures 3 and 4). Locate these ferrite beads within three inches of the SPT5220.

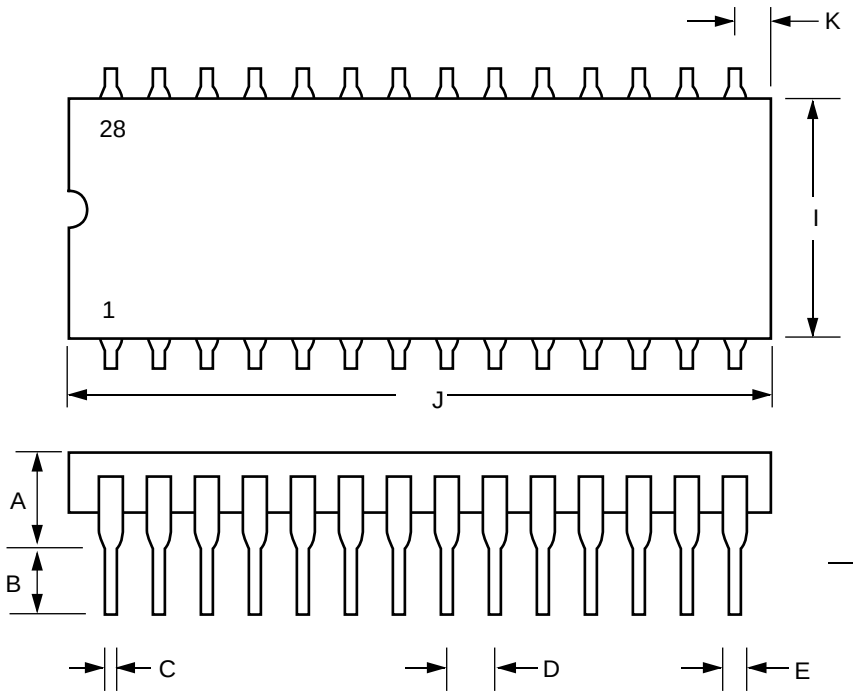
DIGITAL SIGNAL INTERCONNECT

The PCB line between the TTL driver (that drives the SPT5220) and the input to the SPT5220 will have a low impedance source and be terminated with a high impedance. It behaves like a low impedance transmission line so signal transitions will be reflected from the high impedance input of the SPT5220. To reduce ringing caused by transmission line mismatch, shorten the line length or terminate the line. Both serial and parallel termination methods will work, but serial is preferred. Serial termination is achieved by installing a resistor of approximately 50 Ω between the TTL driver output and the SPT5220 digital input.

ANALOG SIGNAL INTERCONNECT

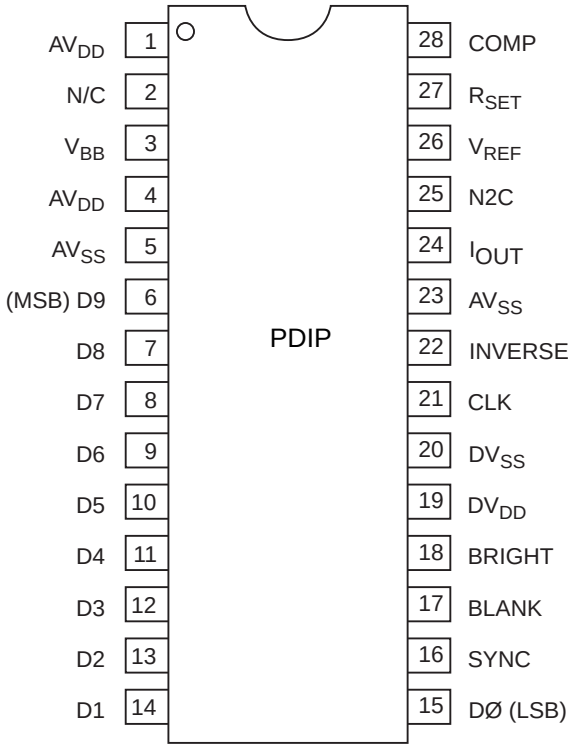
To minimize noise pickup and reflections due to impedance mismatch, locate the SPT5220 as closely as possible to the output connector. The line between the DAC output and the monitor input should be regarded as a transmission line since it can cause problems in transmission line mismatch. Use the double-termination method to avoid these problems. By using the double terminated method, the transmission lines are matched, providing an ideal, nonreflective system.

28-LEAD PLASTIC DIP (PDIP) PACKAGE OUTLINE



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.198 typ		5.08 typ
B	0.117	0.140	3.00	3.60
C	0.014	0.022	0.36	0.56
D		0.099 typ		2.54 typ
E	0.055	0.063	1.42	1.62
F	0.008	0.014	0.20	0.35
G	0.142	0.158	3.65	4.05
H	0.000	0.594		15.24
I	0.523	0.538	13.40	13.80
J	1.439	1.455	36.90	37.30
K		0 .080 typ		2.04 typ
L	0°	15°		

PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
AV_{DD}	Analog Power
N/C	No Connection
V_{BB}	Substrate Power (Connected to AV_{DD})
AV_{SS}	Analog Ground
D9 - D0	Digital Inputs (D9=MSB, D0=LSB)
SYNC	Sync Signal Input (Logic 1 Generates Level)
BLANK	Blank Signal Input (Logic 1 Generates Level)
BRIGHT	Bright Signal Input
DV_{DD}	Digital Power
DV_{SS}	Digital Ground
CLK	Clock Input (TTL-Compatible)
INVERSE	Inverse Signal Input
I_{OUT}	Analog Current Output
N2C	Two's Complement Signal Input (Active Low)
V_{REF}	Voltage Reference (Externally Driven)
R_{SET}	Full-Scale Adjust Control
COMP	Compensation Capacitor

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT5220SCN	0 to +70 °C	28L Plastic DIP

Signal Processing Technologies believes that ultrasonic cleaning of its products may damage the wire bonding, leading to device failure. It is therefore not recommended, and exposure of a device to such a process will void the product warranty.